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# Amplifier performance enhancement methods using positive feedback techniques

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# Amplifier performance enhancement methods using positive feedback techniques

by

**Mezyad M. Amourah**

A dissertation submitted to the graduate faculty

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Graduate College

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This is to certify that the doctoral dissertation of

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Signature was redacted for privacy.

Major Professor

Signature was redacted for privacy.

For the Major Program

To my parents, my wife, and my daughter

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# ABSTRACT

The dramatic growth in the hi-tech sector of consumer market has created many unprecedented challenges in the area of integrated circuits. The present and future communication and entertainment systems including high speed cable and DSL modems, broadband wired and wireless systems, and high definition visual products require very fast and high accuracy amplifiers, data converters and filters. Analog design in the new digital CMOS submicron processes is becoming an economical necessity in the industry. The task of building fast Op-Amp with very high DC-gain is already a very difficult problem, and this task has become more difficult using these new submicron digital processes, where traditional gain enhancement techniques are loosing their ability to deliver amplifiers with sufficient gain. In this work three new methods of implementing the internal positive-feedback to build very high DC-gain amplifiers with very low gain sensitivity to signal swings are presented. Amplifiers proposed in the first method have very high current-controlled gain. A DC gain larger than 100dB is possible without limiting the speed of the amplifier. Amplifiers proposed in the second method exhibit both enhanced speed, i.e., unity gain frequency, and enhanced gain. Amplifiers proposed in the third method have self-adjusting gain without extra control block. An implementation of a 3 bit multiplying DAC in a 9-bit 165MS/s pipeline ADC built in a

1.8V, 0.21μ digital CMOS process using one of the proposed amplifiers is described. Test results show high gain with very fast settling.

# INTRODUCTION TO AMPLIFIER PERFORMANCE ENHANCEMENT

## 1. General Introduction

The dramatic growth in the hi-tech sector of the consumer electronics market has created many unprecedented challenges in the area of integrated circuits. The present and future communication and entertainment systems including high speed modems, broadband wired and wireless subsystems, and high resolution, definition, visual products require very fast and highly accuracy data converters and filters [1, 2]. Because of the wide spread use of CMOS processes, a wide variety of analog and mixed-signal subsystems have performance that is limited by the settling behavior of a CMOS operational amplifier (Op-Amp). These subsystems include switched capacitor filters, programmable gain amplifiers, algorithmic A/D converters, sigma-delta converters, sample and hold circuits, and pipelined A/D converters [1, 2, 3]. In many applications, the settling behavior of the Op-Amp determines both the accuracy and the speed that can be reached. Fast settling requires single-pole settling behavior and a high gain-bandwidth-product [1, 3]. Moreover, for fast applications, the input and output parasitic capacitances became an important factor that limits the speed of operation. High accuracy requires high DC gain. Analog design in the new digital CMOS submicron processes is becoming an economic necessity in the industry. The task of building fast Op-Amps with very high DC-gain is already a very difficult problem and this task become more difficult using the new submicron digital processes [2].

## 2. Thesis Organization

This chapter will visit traditional methods for enhancing amplifiers performance, mainly speed and gain. The next coming section will review the concept of speed, and investigate speed enhancing methods. Next we will go through a survey of gain enhancement methods, investigate the properties and limits of each one of those methods. An example of positive feedback follows up to declare the concept and to show both advantages and disadvantages of the previous implementations. Finally, a survey of previously reported positive feedback implementations including those appeared under different names like negative conductance and bootstrapping techniques are presented.

Chapter 2 will provide detailed vision of two new methods of implementing the positive feedback technique; the current-controlled and the self-adjusting positive feedback techniques. Several implementations of the proposed techniques on some popular amplifiers, Folded and Telescopic cascodes, are presented. Small signal models, gain formulas are given. Implementations of some of the proposed amplifiers in switched capacitor implementations with simulation results are provided. Finally test results for an implementation of the self-adjusting positive feedback amplifier in a pipelined ADC are presented to verify the applicability and the advantages of the proposed structures.

Chapter 3 will present new amplifier architectures that have both speed and gain enhancement properties. Two new techniques were used to boost amplifier's transconductance, gain bandwidth product, without increasing the power dissipation. Positive feedback was employed to simplify the implementation and to boost the DC gain. Proposed structures small signal analysis presented. An implementation of some proposed architectures

in a continuous time $4^{th}$ order high center frequency bandpass filter with relatively high Q-factor is described with simulation results.

Chapter 4 includes the implementation of a very high speed, low supply voltage pipeline ADC suitable for communications and video applications using the self-adjusting positive feedback gain enhanced amplifier. Detailed description of ADC's amplifier, MDAC, voltage comparator, is included. Different simulation and test results that verify the applicability and the power and speed advantages of using digital transistors are presented.

Chapter 5 concludes the whole work. Appendix about layout and testing tips appears at the end of this thesis.

Two Appendixes will present layout and testing tips, and a list of device sizes

## 3. Speed Considerations

As mentioned above the speed of several analog subsystems are mainly limited by the settling behavior of the amplifiers employed in that sub-block. For single-pole amplifiers settling speed is directly proportional to its bandwidth as characterized by the equation.

$$\tau_{sett} = \frac{1}{BW} \tag{1}$$

where $\tau_{sett}$ is the settling time and $BW$ is the bandwidth. The single-pole amplifier bandwidth is approximated by the location of the dominant pole of the amplifier [4,5]. Consider a single-pole output compensated amplifier with an open loop DC gain $A_{ol}$, a dominant pole location $\omega_{p1}$, output impedance $R_{out}$, and a feedback factor $\beta$. The open-loop DC gain is given by

$$A_{ol} = G_m \cdot R_{out} \tag{2.a}$$

where the transconductance is given by

$$G_m = \left.\frac{\partial I_{out}}{\partial V_{in}}\right|_{V_{out}=0} \tag{2.b}$$

The dominant pole frequency is given by

$$\omega_{p1} = \frac{1}{R_{out} \cdot C_{out}} \tag{2.c}$$

the unity gain frequency (UGF) of such a high gain single-pole amplifier is given by

$$\omega_{UGF} = A_{ol} \cdot \omega_{p1} = \frac{G_m}{C_{out}} \tag{3}$$

The frequency dependent gain for the Op-Amp is given by

$$A_{ol}(s) = \frac{A_{ol}}{\frac{s}{\omega_{p1}} + 1} \tag{4}$$

If feedback, with feedback factor β, doesn't load the open loop amplifier and the open loop amplifier doesn't load the feedback network, then the gain with feedback is given by the closed loop transfer function H(s) where

$$H(s) = \frac{A_{ol}}{\frac{s}{\omega_{p1}} + 1 + A_{ol}\beta} \tag{5}$$

This feedback structure is shown in block diagram form in Fig. 1. Pole location of the feedback network is

$$\omega_p \approx -\omega_{p1}\left(1 + A_{ol}\beta\right) \approx -\beta\omega_{UGF} \tag{6}$$

It can be observed from Eq. (6) that the new closed loop pole location, bandwidth, become dependent on the unity gain frequency of the amplifier and on the feedback factor (β).

$$\tau_{sett} = \frac{1}{BW_{cl}} = \frac{1}{\beta\omega_{UGF}} = \frac{C_{out}}{\beta \cdot G_m} \tag{7}$$

where for a given level of settling, the proportionality constant for the open-loop and closed-loop amplifiers are the same. It follows from Eq. (7) that we can enhance the speed of the closed loop amplifier either by increasing amplifier transconductance ($G_m$) or the feedback factor ($\beta$), or by reducing the total output capacitance.

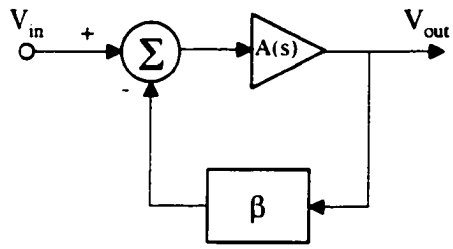



Fig. 1 Amplifier in a closed loop form

The transconductance of the Op-Amp, in general, is proportional to the transconctance of some transistor ($g_{mi}$) at the input stage, and since $g_{mi}$ is proportional to the transistor width to length ratio, and is also proportional to the current passing thru that transistor, the speed can be enhanced either by increasing transistor W/L ratio or by increasing the biasing current thru that transistor [5]. However, increasing the W/L ratio at a constant bias current will lead to reduced input signal swing and to increased parasitic capacitance at the input. On the other hand, increasing the biasing current with a fixed W/L ratio will lead to increased power dissipation. Increasing $\beta$ will have different implications based on the implementation. For example, in the switched capacitor circuit shown in Fig. 2 [4],

$$\beta = \frac{C_f}{C_s + C_f + C_{pr}} \tag{8}$$

Increasing $\beta$ results in a reduction of the closed loop gain. Parasitic capacitance at the input and output nodes are of considerable concern for high speed applications where the

amplifiers require large power dissipation, large transistors, and where the transistor parasitic capacitances start to become significant when compared to the sampling and feedback capacitances.

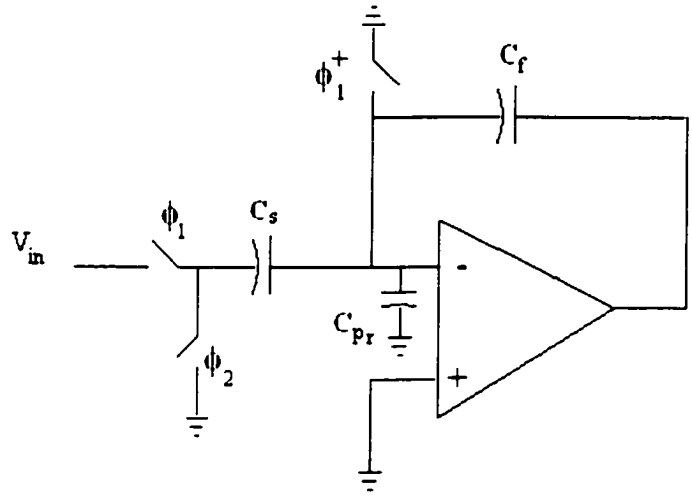



Fig. 2 Typical switched capacitor circuit.

A method that can be exploited to enhance an amplifier transconductance and thus enhance the speed without increasing the power dissipation is by transforming the transistors in the active load or in the cascodes to amplifying transistors. The idea is described in detail in Chapter 3. A modest but yet useful reduction of the parasitic capacitance at the amplifier output can be realized by chopping the active area around the contacts as shown in Fig.3. This technique is used in the amplifier discussed in Chapter 4.

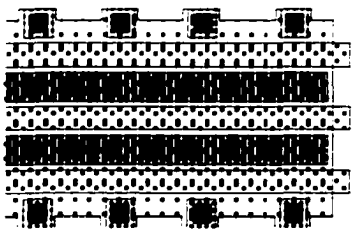


Fig. 3 Chopped-diffusion transistor-layout pattern.

## 3. Gain and Accuracy Considerations

The accuracy that can be reached in many useful systems is directly related to the amplifier open loop gain. For example, in a switched capacitor sample and hold circuit the gain error of the sampler is inversely proportional to amplifier's open loop DC gain [4]

$$G_{error} \approx \frac{1}{1+\beta \cdot A_{ol}} \tag{9}$$

where β is the feedback factor. For filter applications the integrator phase error is inversely proportional to the operational amplifier gain [6]. It is desirable to get higher DC gain for better accuracy and linearity of the feedback network.

### 3.1 Survey of Gain Enhancement Techniques

It follows from Eq. (2.a) that we can boost the gain of a single pole high output impedance amplifier either by enhancing the amplifier transconductance or by enhancing the amplifier output impedance. Other techniques such as cascading several amplifier stages or exploiting the exponential nature of the transistor characteristics in the weak inversion region have also been proposed for enhancing the DC gain [5,7]. Most of the reported techniques that can be used to enhance amplifier gain summarized in Fig. 4.

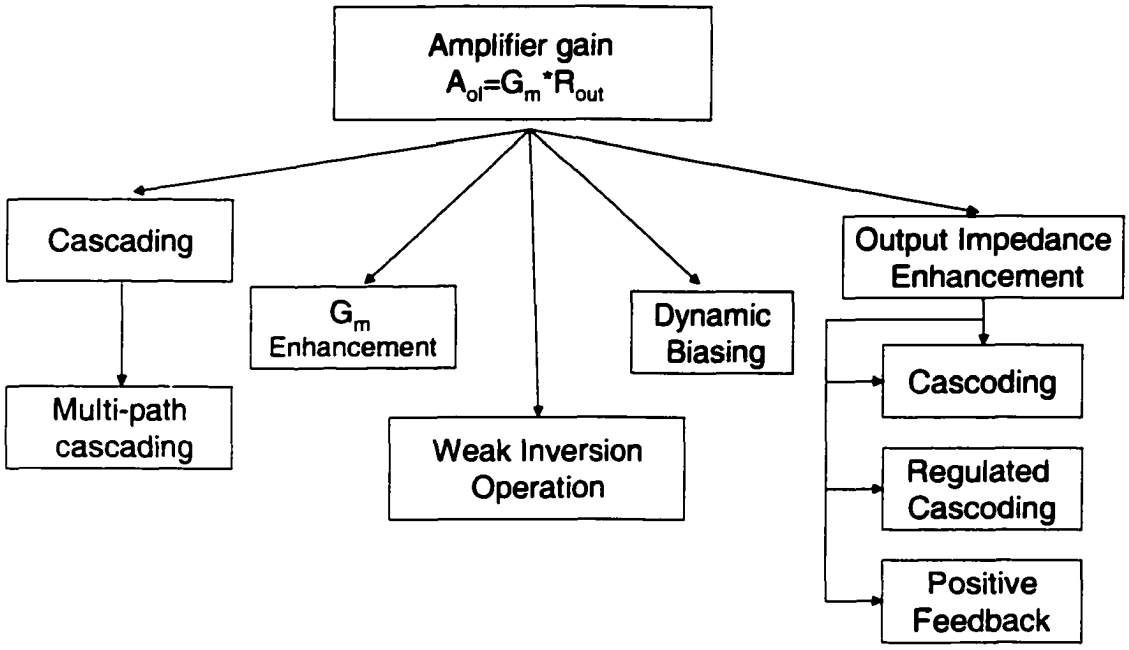



Fig. 4 Gain boosting techniques

Enhancing the gain by boosting the amplifier transconductance is widely used but becomes impractical in very high gain applications because the transistor transconductance is proportional to the square root of the biasing current, assuming fixed W/L ratio, as follows from the square low model.

$$g_m = \mu \cdot C_{ox} \frac{W}{L}(V_{gs} - V_t) = \sqrt{2 \cdot \mu \cdot C_{ox} \frac{W}{L} \cdot I_{ds}} \tag{10}$$

where $\mu$ is the channel mobility, $C_{ox}$ is the gate oxide capacitance density, $V_t$ is the threshold voltage, and $V_{gs}$ and $I_{ds}$ are the quiescent gate-source voltage and drain-source current respectively. So increasing the gain by a factor of two will cost a power penalty by a factor of four.

Cascading of multiple amplifying stages is an attractive approach for enhancing the gain However, due to the required compensation for stable operation, this imposes a severe

speed penalty. For these and other reasons, it is uncommon to see the industry adopting cascades of more than two stages. Several resources have been investigating cascading with a multi-path compensation [8], [9]. However, those multi path structures suffer from the pole zero doublets that made their settling very slow.

An interesting technique to control pole and zero locations is being investigated [9], but it is yet to be experimentally verified for on chip high-speed multi amplifier applications. A basic multi path cascade appears in Fig. 5.

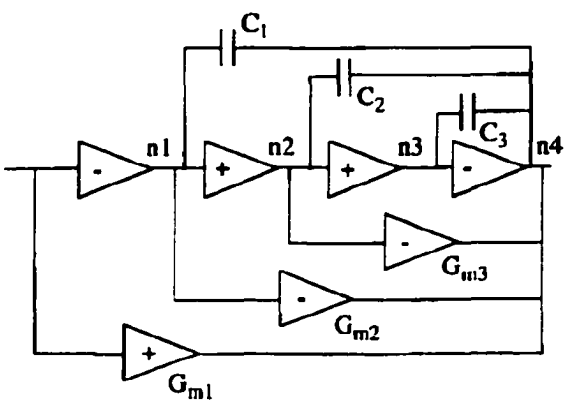



Fig. 5 Basic multi-path cascaded amplifier scheme.

One dynamic biasing technique depends on turning the input transistors into the weak inversion region, where the transistors start to have an exponential relationship between the input voltage and output current, $I_{ds}=I_o exp(V_{gs}/\xi V_t)$.

This is similar to the I-V relationship of the Bipolar transistor. This technique can be used to achieve a very high DC gain. Unfortunately the bandwidth of amplifiers that operate in the weak inversion is very limited. To mitigate this concern, dynamic biasing is used to switch the transistors into the strong inversion region while settling. The basic dynamic biasing scheme is shown in Fig. 6 where the transistors in the differential pair start to operate in the

ohmic region, then the saturation region, and while settling they turn into the sub threshold region when the high gain is achieved. Based on Fig. 6, the operation starts by discharging the biasing capacitor, and then we turn the amplifier ON by closing $\bar{\phi}$, charging the biasing capacitor. During this period the transistors will pass from ohmic region to sub-threshold region [7]. The main draw back of the dynamic biasing technique is that the current driving capability of transistors in the sub threshold region is extremely low which makes settling very slow.

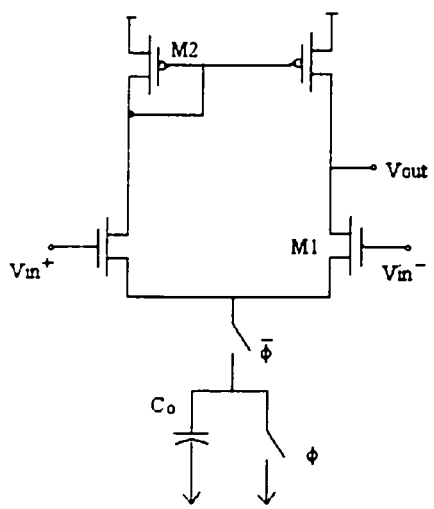



Fig. 6. Implementation of dynamic biasing technique.

Dynamic biasing technique has not been widely accepted in the industry because of this serious draw back. Other important draw back is the fact that charging of the biasing capacitor is dependent on the input signal level thus causing non-linear distortion.

Enhancing the gain by enhancing the amplifier output impedance is the most successful and widely adopted gain enhancement strategy, many times accompanied by a single level of cascading in the same structure. Output impedance enhancement can be

achieved either by using cascoding, regulated cascoding, positive feedback or bootstrapping technique.

Cascoding is a well-known method of enhancing an amplifier output impedance where by stacking or doubly stacking transistors at the output node, the amplifier gain becomes proportional to the square or the cube of the intrinsic transistor gain, $g_m/g_o$ [4,5]. One level of cascoding doesn't provide sufficient DC-gain for many applications. Double and higher level cascoded amplifiers have very limited output swing, and are consequently not applicable to use with low supply voltages. In order to gain more signal swing in cascoded structures it is common practice to fold the cascode. As we go deep in sub-micron processes, the intrinsic transistor output resistance becomes smaller and smaller which limits the advantage of cascoding. Cascoding affects the amplifier DC gain thru changing the effective output impedance, but has no effect on its transconductance and a minimal effect on the unity gain frequency [5]. Cascode, folded, and the double cascode structures are shown in Fig. 7.

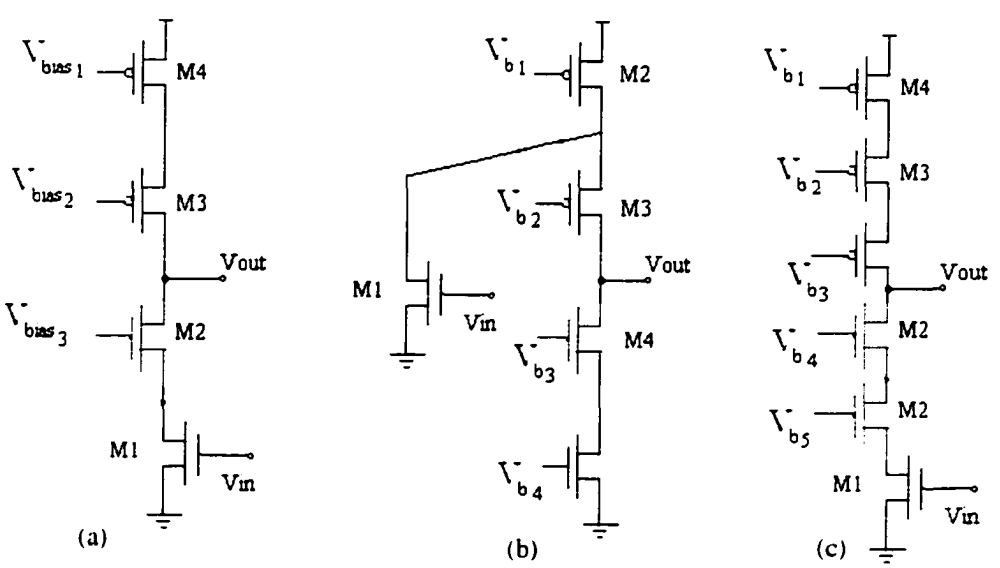



Fig. 7 Cascoded amplifiers. (a) One level cascoding. (b) Folded. (c) Double cascode.

The cascoded gain boosting technique, also known as regulated cascoding, is one of the most successful ways of boosting amplifier gain without seriously limiting the high frequency performance if designed carefully [3,4,5]. Regulated cascoding depends on the existence of at least one level of cascoding. An extra amplifier used in a negative feedback loop as shown in Fig. 8 is used to keep the drain-source voltage across the input cascoded transistor as stable as possible irrespective of the output voltage. The added amplifier boosts the cascode output impedance by a factor, approximately, equal to its open loop gain [3,4] as given by

$$R_{out,reg\_cascode} = (1 + A_A)R_{cascode} \approx g_{m1} \cdot r_{ds1} \cdot r_{ds2} \cdot (1 + A_A) \tag{11}$$

The boosting amplifier forms an extra feedback loop and adds poles and zeros to the final amplifier characteristics which in general will exhibit a pole-zero doublet. This will affect amplifier settling, making it slower. Added amplifiers can be simple common source amplifiers or can be some thing else like cascoded or cascaded structures.

As the semiconductor industry moves toward using the new digital CMOS processes cascading, cascoding, and gain-boosting techniques loose their ability to provide very high DC gain operational amplifiers because digital transistors have high output conductances, and those techniques are dependent upon low output conductances. Expensive solutions like using special analog friendly devices can be used to partially overcome this obstacle.

A technique that can be used to get a high DC gain, named the bootstrapping technique, is based upon using a form of positive feedback in the implementation [10], so the discussion of positive feedback below applies equally to this technique. A simple implementation of the bootstrapping technique is shown in Fig. 9. However, this technique was not proven by test results to be practical and capable of providing high DC gain.

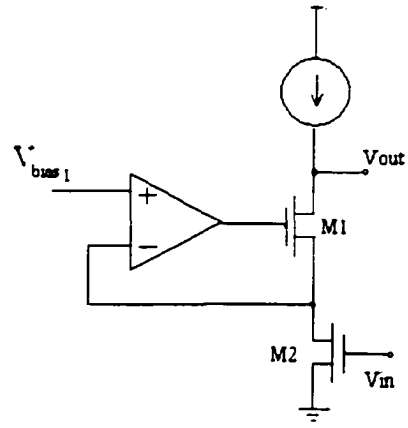



Fig. 8 Regulated cascode gain boosting technique.

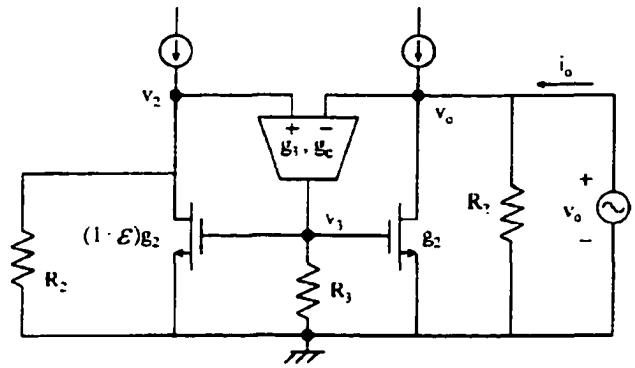


Fig. 9 Amplifier with bootstrapping gain enhancement technique.

## 3.2. Introduction to Positive Feedback Schemes

The concept of applying positive feedback, also known as negative conductance, to enhance the open loop amplifier DC gain was proposed in several publications [6,11]. Most of the proposed structures share the common characteristic of generating a negative resistance by feedback from the output node that is used to compensate some positive resistance at the output to enhance the DC gain. By applying the positive feedback technique, achieving a large DC gain becomes partially dependent on matching of parameters of different transistors that are involved in the positive feedback. A simple example that

illustrates the positive feedback implementation was discussed by Allstot [11]. Cross-coupled active-load PMOS transistors are applied to a simple differential pair as shown in Figure. 10.a. The negative conductance, $-g_{m3}$, generated by the cross coupling is used to boost the DC gain. The small signal model is shown and simplified in Fig. 10.b. A small signal analysis shows that the DC gain of the amplifier, the differential output divided by the differential input, can be written as

$$A_v = \frac{-g_{m1}}{g_{o1} + g_{o2} + g_{o3} + g_{m2} - g_{m3}} \tag{12}$$

If $g_{m3}=g_{o1}+g_{o2}+g_{o3}+g_{m2}$, then the amplifier will exhibit an infinite DC gain. Note that no additional nodes or poles are added with the positive feedback. However, to get the very high DC gain, we need almost perfect matching mainly between $g_{o1}+g_{o2}+g_{o3}+g_{m2}$ and $g_{m3}$.

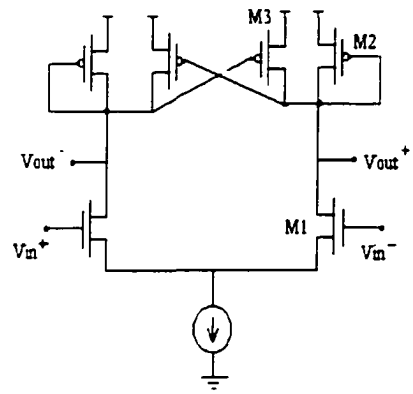
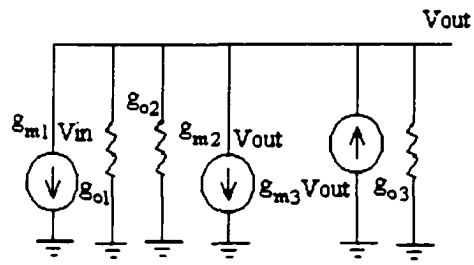



Figure 10.a Regular Differential pair with positive feedback.




Figures 10.b Small signal model, simplified model.

As stated above, previous positive feedback implementations have suffered from two problems. First is a strong dependence of the amplifier's gain on different transistor parameter matching where none of those transistors have controllable or self-adjusting parameters [6], [11]. Second, the high gain sensitivity to output signal-swing. The amplifier transfer function will have a denominator of the form of $(\Sigma g_x - \Sigma g_y)$ where $g_y$ and $g_x$ terms can be the transconductance, or the output conductance of a transistor but most importantly the difference of the two sums must be much smaller than either of the sums. We are looking for wide swing operation, the high sensitivity occurs because this large output swing makes gx and $g_y$ strong function of the output signal. Therefore, the DC gain of the amplifier will change dramatically as the output node swings up or down. This problem is not mentioned in the earlier publications.

The tight matching requirement can be relaxed by three methods. First, make at least one of the key matching parameters controllable and establish some type of adaptive control to achieve the required level of matching. Second, use some kind of cascoding such that the amplifier DC-gain is not completely dependent on the perfect matching issue. Therefore, the existence of cascoding will allow more room for the parameters to move in. Third, use some node other than the output node as the input to the negative conductance element with lower signal swing to reduce the parameter dependence upon output signal swing. If a cascode structure is used , a reduction in the sensitivity of the positive feedback can be achieved if the sensing node is taken from the cascode nodes as will be shown in Chapters 2,3, and 4.

## 6. Survey of Previous Work on Positive Feedback Technique

Positive feedback is used in many aspects of circuit design such as oscillator and bandpass filter design. However, the positive feedback technique has been rarely used as a method to boost Op-Amp gain. Most researchers have avoided the concept because of instability concerns. Others preferred to use other names such as negative conductance and bootstrapping technique. Regardless, the concept has received minimal attention in industry.

In 1982 Allstot [11] built a pre-amplifier for precise voltage comparators using the positive feedback technique for gain enhancement. The preamplifier is redrawn in Fig. 11. The positive feedback was generated by cross coupling of active PMOS load transistors. The preamplifier was built with other ADC components in an 8μm CMOS process. Allstat said little about how much gain enhancement is practically achievable, detailed analysis of this amplifier was done by Gregorian where he suggests that practically this configuration can boost the amplifier gain by at most a factor of four [12].

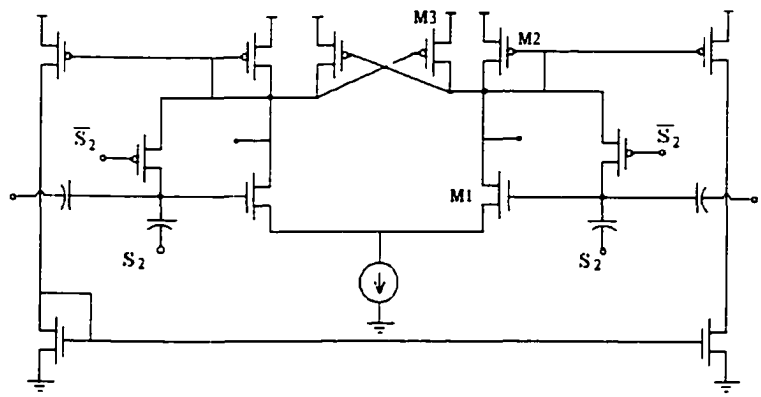



Fig. 11 Pre-Amp with positive feedback

In 1987 Abidi has studied a low supply high gain amplifier under the term of a bootstrapping technique [13]. The amplifier is shown in Fig. 12, and has a DC gain that can be written as

$$\frac{v_{out}}{v_{in}} = \frac{g_m r_o}{1 - \alpha + g_{s2} r_o - \alpha g_{s1} r_o}. \tag{14}$$

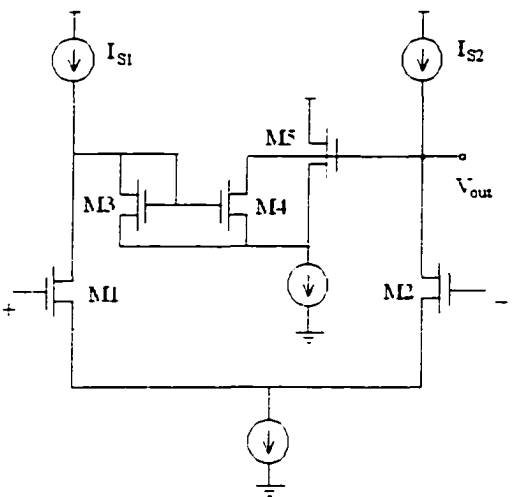



Fig. 12 Boot-strapping technique by Abidi.

In 1988 Labor and Gray used the positive feedback technique to build high gain amplifier, which was used in the integrator, for a high Q-factor switched capacitor filter. This was the first sophisticated amplifier with positive feedback [6]. The amplifier is shown in Fig. 13. In this work the authors assured that regardless of the impedance mismatch, and even if the amplifier's open loop pole moves to the right half plane, the closed loop amplifier will be practically stable whenever enough negative DC feedback is provided by the external β network. The amplifier was implemented in a 3μm CMOS process with a 5V supply. The measured gain was 80dB, but very sensitive to temperature and process variations [6].

In 1989 Nuata and Seevinck used the positive feedback technique to enhance the DC gain of an OTA actually a pseudo-differential OTA that was imbedded in a VHF filter [14].

In there application high gain was required to get excellent linearity. The OTA is shown in Fig. 14. The same OTA was re-used again by Nuata in 1992 to build in a monolithic form. More detailed analysis was done [15]. The OTA was fabricated in a 3μm CMOS process using a 10V supply. The OTA showed a DC gain of 40dB. The OTA gain was given by

$$A_v = \frac{gm_d}{g_{out}} = \frac{gm_d}{\frac{3}{r_{ds}} + gm_4 - gm_3} \qquad gm_d \approx gm_3 \approx gm_4$$

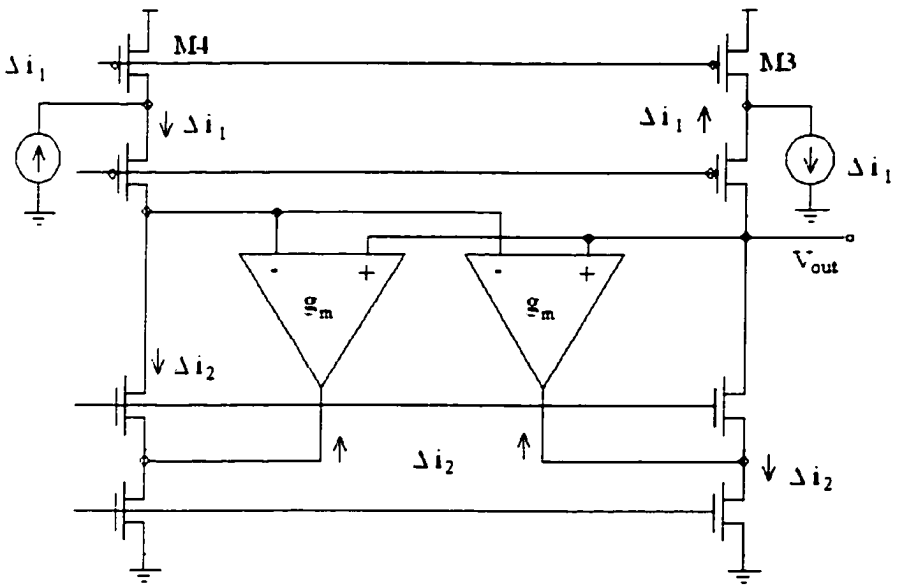



Fig. 13 Amplifier with positive feedback by Labor et al.

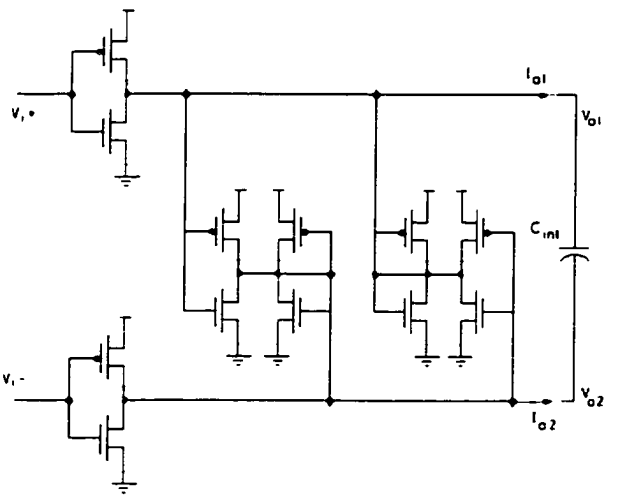



Fig. 14 A pseudo-differential OTA by Nuata.

In 1991 Nakamura et al. built a current based positive feedback amplifier. The amplifier was based on the folded cascode structure as shown in Fig. 15. The amplifier was fabricated in a 2μm CMOS process and tested with 5V supply. The amplifier showed an 84dB DC gain compared to 78dB for the non positive feedback counter part [16]. The gain enhancement was within 6dB range which is a poor improvement compared to the increased power dissipation and the increased complexity of the structure.

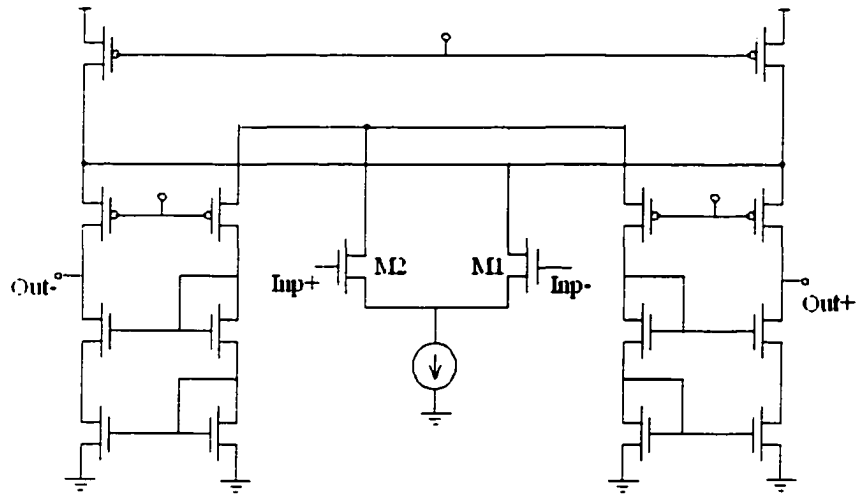



Fig. 15 Current based Postive feedback Amplifier by

In 1997 Lahiji et al. used the positive feedback technique to boost the gain of a bipolar-transistor amplifier. The simplified amplifier is shown in Fig. 16. Simulations showed 160dB gain. No comment was made regarding the sensitivity of the gain to different factors [17].

Finally in 2002 Yan and Geiger reported an amplifier with negative conductance gain enhancement where the amplifier was built using the AMI 0.5μm process. The amplifier gain is dependent on matching of the output conductances of different transistors. The amplifier is shown in Fig. 17. The amplifier transfer function is given by

$$A_v(s) = \frac{v_o}{v_i} = \frac{-g_m}{sC_L + g_{ds} + 1/R_n} \quad \text{where} \quad R_n = \frac{-1}{g_{ds}} . \tag{15}$$

The authors reported a DC gain of 80dB for 50mV output swing, the gain drops to 60dB for output swing of 240mV [18]. This was the first publication that reflects the gain sensitivity to output signal swing.

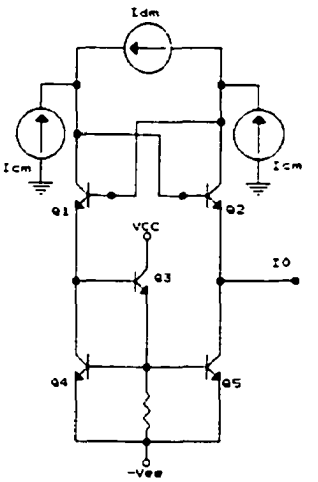



Fig. 16. Bipolar-transistors amplifier simplified schematics by lahiji et al.

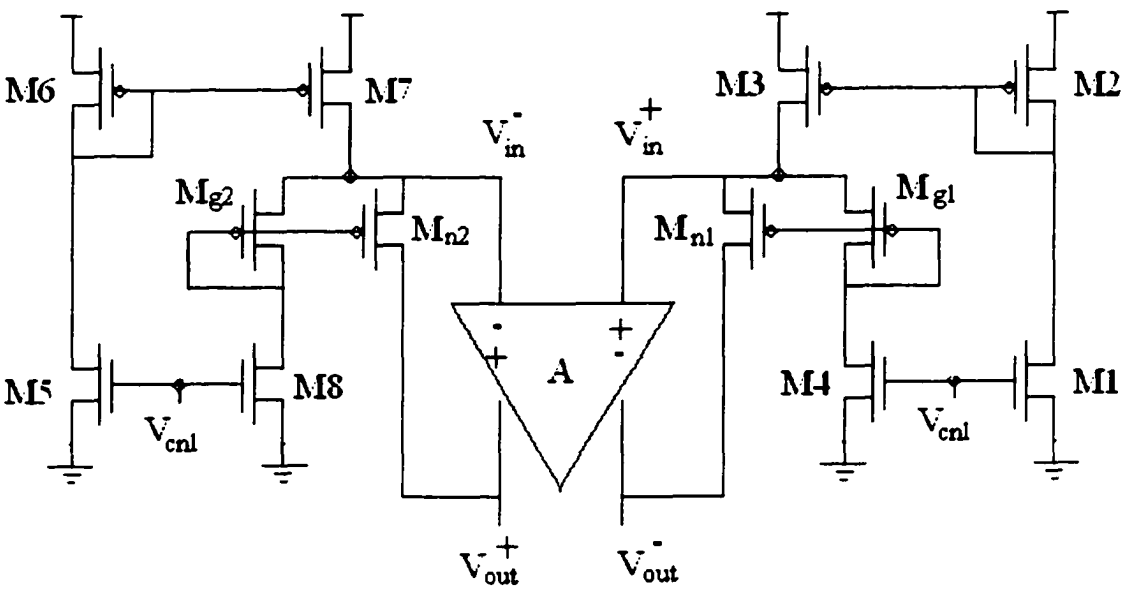



Fig. 17. Amplifier with negative conductance gain enhancement by Yan et al.

## 7. Summary

In this chapter the importance of the signal processing blocks, and the amplifiers in specific are emphasized. The basic amplifier characteristics are visited. Issues related to amplifier speed definition and enhancement methods were highlighted. Amplifier's gain definition and enhancement techniques were reviewed. A wide survey on the positive feedback technique previous implementations is performed. In the next chapters new strategies of implementing the positive feedback technique to boost DC gain and unity gain frequency are presented.

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# A HIGH GAIN STRATEGIES USING POSITIVE-FEEDBACK GAIN ENHANCEMENT TECHNIQUE

A paper to be submitted to the IEEE Transactions on circuits and systems

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## Abstract

Two new techniques that use internal positive-feedback to build very high DC-gain amplifiers are presented. Amplifiers proposed by first technique have controllable gain and don't require perfect matching of transistors to achieve the very high DC gain. An implementation of a sample and hold circuit constructed using the first proposed technique is described. Simulation predicts a DC gain larger than 100dB is possible without limiting the speed of the amplifier. Amplifiers proposed by the second technique have self-adjusting gain property. An implementation of a 3 bit MDAC in a 9-bit pipeline ADC built in a 1.8V, 0.21μ digital process using one of the proposed amplifiers is described. Test results predict high gain with very fast settling.

## 1. Introduction

High accuracy, good linearity, and high speed are the three most important properties of many useful analog and mixed-signal circuits and systems. Invariably, the speed performance in these circuits is limited by the settling behavior of a CMOS operational amplifier (Op-Amp). Included in this class of useful circuits are switched capacitor filters, algorithmic A/D converters, sigma-delta converters, sample and hold circuits, and pipeline A/D converters [1], [2], [3]. The settling behavior of the Op-Amp has a direct impact on both

the accuracy and the speed that can be achieved. Continual wisdom teaches fast settling requires single pole settling behavior and a high gain-bandwidth-product (*GB*) [1,2,9]. In high-speed applications, the input and output parasitic capacitances also limit the speed of operation. High accuracy and good closed loop accuracy requires a high DC gain.

High performance analog and mixed–signal design in state of the art digital CMOS processes has become an expectation of the industry for nearly the past two decades. The task of building fast Op-Amps with a very high DC-gain is a difficult problem and this task has become much more difficult in the submicron digital processes [3]. There is a little in the literature that shows promise for allowing designers to meet these expectations in processes with feature sizes smaller than 0.1μm. The high GB and fast settling with short channel devices have been approached by designers by biasing the critical devices at high current levels [2,5,6]. The high DC gain of the Op-Amp has been approached by one or more of the following techniques; cascading of gain stages, applying dynamic biasing, or using output impedance enhancement.

Cascading two stages or more can result in a very high DC gain, however, the regular compensation for stable operation will seriously limit the high frequency performance [1,2]. For these reasons cascading of three or more stages is not a common practice in the industry. A related cascaded approach relies upon alternative compensation circuits and is termed multi-path nested or feed-forward cascade these structures are noted for challenging problems with achieving exact pole-zero cancellation [7]. Without precise cancellation the existence of pole-zero doublets makes settling very slow.

The second method, dynamic biasing, was reported to combine high DC gain and a fast settling [4]. However, in dynamically biased amplifiers, during the settling period the

critical active devices operate in the weak inversion region to enhance the DC gain but the settling becomes slow. Moreover, a single stage dynamically biased amplifier may not provide sufficient gain and cascading them is difficult [5]. Dynamically biased amplifiers have limited acceptance because of this disadvantage [1,2].

The third method of enhancing the DC-gain of the Op-Amp is to increase its output impedance. This task was performed either by cascoding, using gain-boosting (often termed regulated cascoding) techniques or by using negative conductance positive feedback. A related technique termed boot strapping is another form of the positive feedback technique [8]. The cascoding approach is well-known and has been widely used method of gain enhancement by the industry for the past decade. With cascoding the amplifier gain becomes proportional to the square or the cube of the intrinsic transistor gain, $g_m/g_o$. One level of cascoding usually doesn't provide sufficient DC-gain. In more recent digital processes, the double cascoded amplifier has very limited output swing, and is not applicable to low-voltage circuits. Enhancing amplifier gain by the gain-boosting technique is one of the most successful ways of boosting amplifier gain without seriously limiting the high frequency performance [2]. However, the boosting amplifiers do add poles and zeros to the amplifier transfer function and will create new local feedback loops in the structure. This will generate pole-zero doublets, which will slow the settling of the amplifier. As the industry move to deep submicron processes, native transistors show higher and higher output conductances which makes the previous techniques, cascading, cascoding, and gain boosting, less and less capable of providing the high DC gain that is needed. The easiest solution and a solution that has been widely adopted is the use of special processes that provide "analog friendly" devices. These analog friendly devices have longer channels, lower threshold voltages, and

worse gate leakage when compared to the native digital transistors. Longer channel lengths and lower threshold voltage in larger transistor sizes and larger parasitic capacitances thus slowing the step response. Analog friendly devices have longer time to market and often exhibit big differences in performance from one foundry to another [3]. The dominant limitation of using analog friendly devices is, however, the increased processing costs and need for multiple supply voltages. The third method of enhancing the output impedance is by using the positive feedback, or the negative conductance/transconductance technique. Positive feedback offers potential for obtaining a very high DC gain without adversely affecting the high frequency performance. In particular, positive feedback has the potential of providing high gain using only digital transistors. Most of the positive feedback implementations that have been proposed suffer from two limitations. First is a strong dependence of the amplifier gain on precise transistor matching [1,2,4]. The second is high gain sensitivity to the output signal swing. There is also a previous and un-narrated concern about potential instability in the open loop amplifier causing stability problems in feedback circuits that use unstable open loop amplifier. The strong amplifier gain dependence on transistor matching occurs because the gain depends on matching between different types of devices parameters that are inherently weakly correlated and highly variable from one process to the next. The high sensitivity to output signal swing is caused by the fact that the positive feedback is invariably taken from the output node that has a large swing. For applications requiring wide output swing operation, this connection will make the gain a strong function of the output signal level. Therefore, the DC gain of the amplifier will drop sharply as the output node voltage swings up or down. This signal-swing problem was not addressed in the early publications. Finally it must be recognized that effective use of the

positive feedback technique may generate an Op-Amp with a dominant pole in the right half plane. This is, however, not a problem in most applications since use of the amplifier in a loop with negative feedback will guarantee stability as will be shown in the next section. The positive feedback method, in contrast to the other methods of enhancing output impedance, holds potential for building fast amplifiers with a very high DC gain suitable for operation in all-digital low voltage processes.

Finally, for simplicity during the rest of this work, even though, for small signal analysis only one half of the equivalent small signal circuit will be shown, all derivations of gain and transconductance, for differential structures, are for differential input differential output signals.

## 2. Introduction to Positive Feedback Schemes

The concept of applying positive feedback, also known as negative conductance or transconductance compensation, to enhance the open loop amplifier gain has been proposed in several publications. Most of the proposed structures share the common characteristic of generating a negative conductance by internal feedback of a signal from the output node that is used to compensate for the inherent positive conductance at the output to achieve the very high DC gain. To illustrate the basic positive feedback gain enhancement technique, consider the cross-coupled active-load PMOS transistors used to compensate the output conductance of a simple differential pair as shown in Fig. 1. A negative transconductance, $-g_{m3}$, is generated by the cross coupling of transistors $M_3$ and $M_3'$. The small signal model is shown in Fig. 2. A small signal analysis shows that the DC gain of the amplifier can be written as

$$A_o = \frac{V_{out}}{V_{in}} = \frac{-g_{m1}}{g_{o1} + g_{o2} + g_{o3} + g_{m2} - g_{m3}} \qquad (1)$$

If the transistor $M_3$ is sized such that

$$g_{m3}=g_{o1}+g_{o2}+g_{o3}+g_{m2} \tag{2}$$

then the amplifier will exhibit an infinite DC gain. Note that no additional nodes or poles are added with the positive feedback. However, to get the very high DC gain, nearly perfect matching between $g_{o1}+g_{o2}+g_{o3}+g_{m2}$ and $g_{m3}$ is required. The perfect matching over process variations, temperature variations and signal swing is very difficult to achieve.

The stability of feedback amplifiers using a positive feedback Op-Amp does deserve consideration because of the wide spread concern about this problem. If $C_l$ is the total load capacitance on the output node $V_{out}^+$ in the amplifier of Fig. 1, then the frequency dependent gain is given by the expression

$$A_v = \frac{-g_{m1}}{sC_L + (g_{o1} + g_{o2} + g_{o3} + g_{m2} - g_{m3})} \tag{3}$$

This amplifier gain can be written as

$$A_v(s) = \frac{GB}{s - \omega_{po}} \tag{4}$$

where

$$GB = |A_o \cdot \omega_{po}| \tag{5}$$

where $A_o$ is given by (1) and where the pole of the Op-Amp, $\omega_{po}$, is given by

$$\omega_{po} = [g_{m3} - (g_{o1} + g_{o2} + g_{o3} + g_{m2})] / C_L \tag{6}$$

It is apparent from (6) that the pole of the open loop Op-Amp will move into the RHP if

$$g_{m3} \rangle g_{o1} + g_{o2} + g_{o3} + g_{m2} \tag{7}$$

Although the specific relationship between the $A_o$ and $\omega_{po}$ and the device model parameters for the circuit of Fig. 1 is defined by (1) and (6). The functional form of (5) is characteristic

of positive feedback amplifiers in general. A negative feedback network using a positive feedback operational amplifier characterized by (5) is shown in Fig. 3. A standard analysis of the feedback amplifier gives the closed-loop transfer function

$$H(s) = \frac{GB}{s - \omega_{po} + \beta \cdot GB} \tag{8}$$

From (8) it is apparent that the closed loop pole location is given by

$$\omega_p = \omega_{po} - \beta \cdot GB \tag{9}$$

It follows from (9) that the closed loop amplifier will be stable provided

$$\omega_{po} < \beta \cdot GB \tag{10}$$

For practical amplifier circuits, the magnitude of the dominant open-loop pole, irrespective of whether it is in the LHP or the RHP, must satisfy the relationship

$$|\omega_{po}| << \beta \cdot GB \tag{11}$$

It thus follows from (10) and (11) that the closed loop amplifier will be stable independent on whether the open loop amplifier is stable or unstable wherever (11) is satisfied. Note (10) not only shows the closed loop amplifier will be stable for all practical amplifier circuits irrespective of the stability of the open-loop amplifier, it also shows the closed-loop pole will lie far in the LHP on the negative real axis.

## 3. Conceptual Description of the Proposed Positive Feedback Techniques

### 3.1 Low Sensitivity Current-Controlled Positive Feedback Technique

We propose constructing new amplifiers by applying controllable positive-feedback to several standard cascoded amplifiers. By applying a controllable positive feedback in combination with cascoding, transistor-matching requirements are relaxed. The positive

feedback signal used to enhance the DC-gain is derived from the extra nodes created by the cascode. Since the signal swing at the cascode nodes is much smaller than the output signal swing, this approach will considerably reduce the effect of the output voltage level on the amplifier gain. Figures 4.a and 4.b show the implementation of the current-controlled transconductance cross-coupled transistors to traditional folded cascoded, and telescopic amplifiers. Fig. 4.c, and Fig. 4.d show the possibility of realizing high DC gain amplifiers, high speed with the rail to rail option for the amplifier shown in Fig4.d. All of the amplifiers presented here are fully differential. Common mode feed back circuits, and biasing circuits are not shown for simplicity. We will concentrate on the amplifier shown in figure 4.a. The other amplifiers in Fig.4 exhibit similar properties. The gain of the amplifier shown in Fig. 4.a can be controlled using replica-biasing scheme. The amplifier shown in Fig. 4.a has a small signal model that is shown in Fig. 5. Ignoring the bulk effect, for simplicity of expressions and considering differential input differential output relation, this structure has an open-loop gain, $A_v$, of the form.

$$A_v = -g_{m1} \Big/ \left( \frac{g_{o3}\left(g_{o1} + g_{o2} + g_{o6} - g_{m6}\right)}{g_{m3}} + \frac{g_{o4}g_{o5}}{g_{m4}} \right) \tag{12}$$

Assuming that $g_{m3} \approx g_{m4}$, $g_{03} \approx g_{04}$, and $g_{o6} << g_{o1,2}$ the voltage gain can be rewritten as

$$A_v = \frac{-g_{m1} \cdot g_{m3}}{g_{o3}\left(g_{o1} + g_{o2} + g_{o5} - g_{m6}\right)} \tag{13}$$

Equation (13) shows that the DC-gain of the amplifier can be infinite as gm6 approaches $g_{o1}+g_{o2}+g_{o5}$. Looking back to Figure 4.a we see that $g_{m6}$ is fully programmable by controlling the tail current, which allows us to overcome the process and temperature variation effects. Observing voltages $V_x^+$ and $V_x^-$ we notice that they experience very small swings compared

to $V_{out}^{+}$ and $V_{out}^{-}$ since $V_x=V_{out}/(g_{m3}/g_{o3})$. For example in our design the intrinsic transistor gain of $M_3$ is slightly larger than twenty, $g_{m3}/g_{o3}>20$. So if the output voltage have a swing of one volt, $V_{out}=V_{cm}\pm 250mV$, then voltage $V_x$ experience a swing that can be written as $V_x=V_{cm}\pm 12.5mV$. Therefore, $g_{m6}$ is not a strong function of the output voltage level. The amplifier shown in figure 4.c can be applied where a moderate gain is required with moderate output impedance. Under the approximation of $g_o<<g_m$, voltage gain, $A_v$, can be written as

$$A_v = \frac{-g_{m1}\cdot g_{m2}}{(g_{m3}\cdot g_{m2} - g_{m4}\cdot g_{o2})} \tag{14}$$

As $g_{m4}$ approaches $(g_{m2}\cdot g_{m3})/g_{o2}$ we will end up having very high DC-gain. This amplifier shows very high bandwidth. Note that $g_{m4}$ is fully controllable. Finally the opamp shown in Figure 4.a is applied to a sample and hold circuit with sampling frequency of 50MHz. Simulation shows high settling speed as will be shown in the next section.

Gain control can be done in many ways. One straight forward way is to build a replica scheme, sense the gain of that replica amplifier and use it to control the desired amplifier gain. The extra replica amplifier don't need to consume the same power as the amplifier in use, it can be a scaled version. Moreover, for several applications were multiple amplifiers set close to each other on the same substrate, one replica amplifier can be used to control the gain of all the amplifiers. Gain control circuit can run at a very low speed since it is controlling biasing parameters. A simple control circuit appears in Fig. 6. We need to control both tail current sources in complimentary way such that the total current stays fixed. Gain control depends on the fact that as the pole switches from left half plane to right half plane, amplifier outputs switch polarity. For example in case of amplifier shown in Fig. 4.a, amplifier's gain can be written as

$$A_v = \frac{-g_{m1} \cdot g_{m3}}{g_{o3}(g_{o1} + g_{o2} + g_{o5} - g_{m6})} \tag{15}$$

First we reset the amplifier in a closed loop form using the auto-zero technique to eliminate the offset voltage effect then we open the loop. Next we start to change amplifier's tail currents. Always we start from a situation where $g_{m6}$ is small, so replica amplifier differential output will be positive, controlling the discrete integrator to increase its output by a very fine step. This increase in integrator's output will increase the current flowing thru transistor $M_6$, and reduce that through $M_1$, which increases $g_{m6}$ and reduces $g_{o1}$. This behavior continues until $g_{m6}$ becomes larger than the sum of $g_{o1}$, $g_{o2}$, and $g_{o5}$, once this happens the amplifier differential output becomes negative and we stop the operation of the control circuit and we modify the biasing of the other amplifiers. In this technique, for best results, we need to short together the two amplifier outputs every time before we change the control voltage. In our design this action is done inside the opamp by the common mode feedback circuit (CMFB).

### 3.2 Low Sensitivity Self-Adjusting Positive Feedback Technique

Again we propose here constructing new amplifiers by applying positive-feedback to several standard cascoded amplifiers. By applying a self-adjusting positive feedback in combination with cascoding transistor matching requirements are relaxed. The positive feedback signal used to enhance the DC-gain is derived from the extra nodes created by the cascode to reduce the effect of the output signal level on the amplifier gain. Figures 7.a, and 7.b show the application of the proposed positive feedback to traditional telescopic, and folded cascode amplifiers. Amplifiers presented here are fully differential. Common mode feed back circuits, and biasing circuits are not shown for simplicity. We will concentrate on

the amplifier shown in Fig. 7.a. In this work the amplifier shown in Fig. 7.a is implemented using digital transistors in a 1.8V, 0.21μ CMOS process.

The proposed amplifier is constructed using two-stage architecture. The first stage is a telescopic amplifier with positive feedback. The second stage is a simple differential pair as shown in Fig. 7.a. The two stage architecture was chosen because we are looking for wide swing operation of 1.1 $V_{p-p}$ while employing a low supply voltage of 1.8V. The existence of the second stage with the positive feedback being implemented in the first stage will make the gain sensitivity to the signal swing even lower. The first stage of the amplifier has the simplified small signal model shown in Fig. 8. Small signal analysis shows that the first stage has an open-loop gain, $A_v$, of the form;

$$A_v \approx \frac{g_{m1}\cdot(g_{o2}+g_{m2})g_{m3}}{[g_{o1}g_{o3}g_{o4}+g_{o2}g_{o3}g_{o4}+g_{o1}g_{o2}g_{m3}+g_{o3}g_{o4}g_{m2}-g_{o1}g_{o3}g_{m2}]} \tag{16}$$

Assuming that $g_{o1}\approx g_{o4}$, and $g_m >> g_o$, voltage gain can be rewritten as;

$$A_v \approx \frac{g_{m1}g_{m2}g_{m3}}{[g_{o1}g_{o2}g_{m3}+g_{o3}g_{o4}g_{m2}-g_{o1}g_{o3}g_{m2}]} \tag{17}$$

Equation (17) shows that the DC-gain of the first stage becomes very large and from (10) will approach

$$A_v \approx \frac{-g_{m1}g_{m2}g_{m3}}{[g_{o1}g_{o3}g_{o4}+g_{o2}g_{o3}g_{o4}]} \tag{18}$$

as $(g_{o1}\cdot g_{o3}\cdot g_{m2})$ approaches $(g_{o1}\cdot g_{o2}\cdot g_{m3}+g_{o3}\cdot g_{o4}\cdot g_{m2})$. This is comparable to what would be achieved with a double cascode structure that would require the stacking of two additional transistors in each half-circuit. It can be observed from Fig. 7 that the positive feedback in the

differential mode is negative feedback in the common mode. This negative feedback helps the Op-Amp to adjust its biasing condition to maintain the high gain.

It is well known that the channel length modulation causes the transistor output conductance to be larger than zero [9,10]. The transistor output conductance is given by

$$g_{oi}=\lambda_i I_{dsi} \tag{19}$$

where $\lambda i$ is the channel length modulation coefficient and $I_{ds}$ is the common drain current. It thus follows from, $g_{o1}\cdot g_{o2}+g_{o3}\cdot g_{o4}-g_{o1}\cdot g_{o3}\approx 0$, that

$$g_{o1}\cdot g_{o2}+g_{o3}\cdot g_{o4}-g_{o1}\cdot g_{o3}=I_{ds}^{2}\cdot(\lambda_1\cdot\lambda_2+\lambda_3\cdot\lambda_4-\lambda_1\cdot\lambda_3) \tag{20}$$

It is well known that the $\lambda$ parameter is dependent on gate length and is given by the relationship

$$\lambda_i=\frac{1}{L_i}\cdot\frac{\partial X_{di}}{\partial V_{dsi}} \tag{21}$$

where $X_d$ is the gate reduction of the channel due to $V_{ds}$. If it is assumed that $(dX_{di}/dV_{dsi})$ is constant and the same for both N-channel and P-channel devices then setting the rightmost factor in (20) to zero, we obtain the relationship

$$(\lambda_1\lambda_2+\lambda_3\lambda_4-\lambda_1\lambda_3)=\left(\frac{\partial X_{di}}{\partial V_{dsi}}\right)^{2}\cdot\left(\frac{1}{L_1\cdot L_2}+\frac{1}{L_3\cdot L_4}-\frac{1}{L_1\cdot L_3}\right)=0 \tag{22}$$

If we choose the lengths $L_1$, $L_2$, $L_3$, and $L_4$ so that $L_1=L_3$ , and $L_2=L_4$, then setting the rightmost factor in (22) to zero, results in the expression

$$\frac{1}{L_1\cdot L_2}+\frac{1}{L_1\cdot L_2}-\frac{1}{L_1^2}=0 \tag{23}$$

which will be satisfied if

$$L_2=2L_1 \tag{24}$$

Thus, setting $L_2=2L_1$ will result in the gain given by

$$A_v \approx \frac{g_{m1} \cdot g_{m2} \cdot g_{m3}}{[g_{o1}g_{o3}g_{o4} + g_{o2}g_{o3}g_{o4}]} \tag{25}$$

assuming $g_{m1}=g_{m3}$ and substituting from (19),(21) and (24) into (25) we obtain

$$A_v \approx \frac{2g_{m1}^2 \cdot g_{m2}}{3g_{o1}^2 g_{o4}} = \left[\frac{g_{m1} \cdot g_{m2}}{2g_{o1}^2}\right]\left[\frac{4g_{m2}}{3g_{o4}}\right] \tag{26}$$

It can be shown that the gain of the basic cascode without the positive feedback is given by

$$A_v \approx \frac{g_{m1} \cdot g_{m2} \cdot g_{m3}}{[g_{m3}g_{o1}g_{o2} + g_{m2}g_{o3}g_{o4}]} \tag{27}$$

If we assume gm2=gm4 in this structure and the lengths are all the same so that $g_{o1} \approx g_{o3} \approx g_{o2} \approx g_{o4}$, then the basic cascode has gain of

$$A_v = \frac{g_{m1} \cdot g_{m2}}{2g_{o1}^2} \tag{28}$$

Comparing (26) and (28), it follows that the positive feedback and length sizing has resulted in a boost in gain of $(4g_{m2}/3g_{o4})$ which can be quite significant.

Common mode circuit of the first stage can be redrawn as shown in Fig. 9. To see how process variations will affect the quiescent voltages and currents of the circuit, let us consider the strong PMOS case. For this case, the magnitude of $V_{th}$ for the PMOS transistors will be lower resulting in larger $g_{o3,4}$ and $g_{m3,4}$ since transistors $M_3$ and $M_4$ are connected to

fixed bias references. Therefore, both the nodes $V_{out\_T}$ and $V_x$ will be pulled up towards $V_{dd}$. Since the operating point of the transistor $M_2$ is set by the positive feedback connection, and since $M_2$ forms an inverting common source amplifier with source degeneration, then increasing its $V_{gs}$ will turn it on harder increasing $g_{m2}$, $g_{o2}$, and $g_{o1}$. Since $g_{o1,3} \approx 2g_{o2,4}$ this will make the increase in the value of the negative term in the denominator of Eq. (17) able to track the increase of the sum of the positive terms and adjusting the gain. Note that the change in the excess bias of transistor $M_3$ is equal to the change of the excess bias of transistor $M_2$ which helps gm2 and gm3 to track each other under the assumption of fixed voltage at node $V_y$. This negative feedback loop in the common mode circuit, shown in Fig. 9, has large gain and its operation is consistent with the operation of the common mode feedback circuit. Similar arguments can be made for the other process corners. The existence of the extra biasing circuitry, shown in faded color in Fig. 10 has two main functions: First, it defines the quiescent biasing voltage, $V_y$. Second, it helps to fix the voltage of node $V_y$. Observing voltages $V_x^{\pm}$ we notice that they experience very small swings compared to $V_{out}^{\pm}$, since $V_x = V_{out}/(g_{m3}/g_{o3})/G_s$, where $G_s$ is the gain of the common source output stage. For example in our design $(g_{m3}/g_{o3} * G_s) > 200$, so if the differential output voltage has a swing of $1V_{p\text{-}p}$, then voltage $V_x^{\pm}$ will experience less than $5mV_{p\text{-}p}$ swing. Therefore, the feedback is almost unaffected by the output signal level. The two stages amplifier is Miller compensated. Compensation capacitors where connected to the cascode nodes, for simplicity, only one side of the compensation capacitors is shown in Fig. 10.

Finally the amplifier, shown in Fig. 10, is embedded in a 9-bit 1.8V ADC circuit. The ADC was tested at frequencies as high as 82MS/s. Simulation and test results show high speed slewing and settling, with sufficiently high gain.

# 4. Simulation Results

## 4.1 Current Controlled Folded Amplifier with Positive Feedback.

The folded cascoded amplifier with the internal positive feedback, shown in Fig. 4.a, was simulated using CMOS TSMC 0.25u process. The amplifier consumes a total current of 800uA at a supply voltage of 2.5V, and deriving a capacitive load of 500fF. Simulation shows that typically we can get a DC gain of 103.6dB with a unity gain frequency of 278MHz. A comparison between the modified and the traditional folded cascoded is shown in Table 1 where both amplifiers have been simulated with approximately the same power dissipation, the same excess bias on the similar transistors, and the same load capacitance. The table shows that for approximately the same conditions we were able to enhance the DC-gain from 46dB to 103dB, for the same load, and phase margin. Results are shown in Figures 11.a, and 11.b. Moreover, the same amplifier architecture was applied to a switched capacitor sample and hold circuit with two non-over-lapping clocks at frequency of 50MHz with 1nsec separation between the two non-overlapping phases. The circuit is shown in Fig. 12. The amplifier implemented consumes a total current of 3.6mA, and drives a load capacitance of 1pF. The sampling capacitors have a size of 550fF. Simulation results are shown in Fig. 13 a, b. Simulation with parasitics shows that the amplifier was able to slew and settle to an error less than 0.23mV for a 1V peak-to-peak output swing within 3nsec time period, which is equivalent to 11-bit of accuracy.

**4.2 Self-Adjusting Positive Feedback Implementation.**

The telescopic amplifier with the internal positive feedback, shown in Fig. 10, was simulated using Texas Instruments digital CMOS 0.21μ process. The amplifier draws a total current of 8.0mA, has two common mode feedback circuits, and operates with a supply voltage of 1.8V while driving a capacitive load of 1.0pF. Compensation capacitor size, $C_C$, was 400fF, that is a total of 800fF per side. Simulation shows that the amplifier has a DC gain of 81dB with a unity gain frequency of 1.218GHz. A comparison between the modified and the traditional telescopic cascode is shown in Table 1, where both amplifiers have approximately the same power dissipation, the same excess bias on the similar transistors, the same load capacitance, and both were built using only digital transistors. The table shows that we were able to enhance the DC-gain from 63dB to 80dB, for the same load, and phase margin. Results are shown in Fig. 14.a,b. DC sweep shows that the amplifier has a maximum swing of $1.5V_{p\text{-}p}$ with gain higher than 68dB under nominal conditions.

Moreover, the same amplifier architecture was used with a switched capacitor sample and hold circuit that forms a 3-bit MDAC with one redundant bit using two non-over-lapping clocks at frequency in the range 27MHz to 165MHz. The simplified sample and hold circuit is shown in Fig. 16. The sampling unit capacitor has a size of C1=125fF and the MDAC circuit has a gain of 4. Post layout simulation results are shown in Fig. 17.a, b. Simulation shows that the amplifier was able to slew and settle to an error less than 0.2mV for a 1V peak-to-peak output swing within 2.1nsec. Chopped diffusion transistor layout pattern is shown in Fig. 18. Using this pattern we were able to reduce the diffusion parasitic capacitance at the expense of increasing the side-wall-capacitance, which has a much lower

density than the diffusion one. Layout extraction in the case of wide devices shows that we can save 15% to 20% of the parasitic capacitance value using this technique.

## 5. Test Results

The proposed Op-Amp, shown in Fig. 10, was embedded in a 9-bit 1.8V pipeline ADC constructed using 4 stages, each of which is a 3-bit stage. First three stages have 1 bit of redundancy used for digital error correction to relax the requirements for the comparator offsets. MDAC simplified sample and hold circuit was shown in the previous section. The prototype chip is implemented in a 0.21μm, 5 metal layers, double poly, CMOS copper technology. A die photo that includes an ADC channel is shown in Fig.20. The die surface is covered by dummy metal layers. The input/output swing of the MDAC is $1.1V_{p\text{-}p}$. The measured DNL and INL curves are presented in Fig 21. Max DNL and INL at 82MS/s are 0.39LSB and 0.75LSB respectively. The SNR and SFDR at 10MHz input frequency and sampling rate of 82MS/s are approximately 46.8dB and 54dB respectively as shown in Fig. 22.

## 5. Conclusions

Two Positive-feedback techniques were used to enhance the DC-gain of several popular second order amplifiers, without sacrificing the high frequency performance. First technique uses current controlled positive feedback where gain is controlled by a tail current source. The second technique uses a self-adjusting structure where devices in the feedback loop have parameters that track each other. Both techniques show low gain sensitivity to output signal swing, temperature and process variations. These techniques are applicable to

low-voltage digital processes as proved by the implementation of the second technique in a fast 9-bit ADC. Test results verified the concept.

## 6. References

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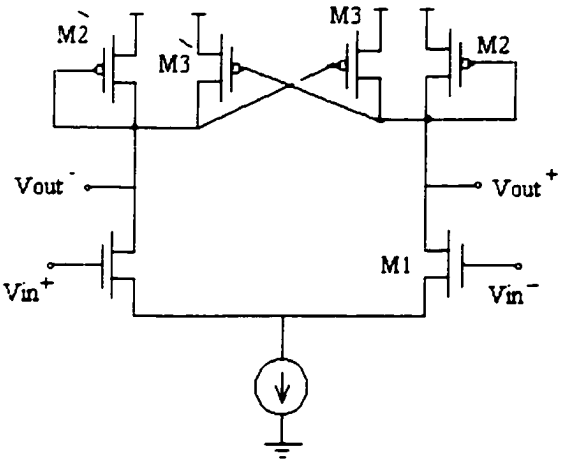



Fig. 1 Differential pair with positive feedback gain enhancement.

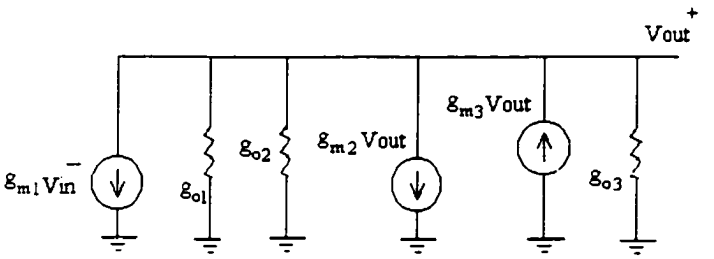



Fig. 2 Small signal model for one half of the positive feedback amplifier.

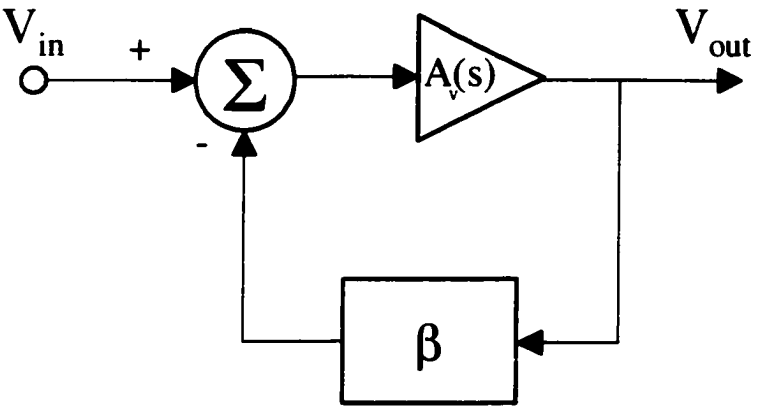



Fig. 3 Amplifier in a negative feedback loop.

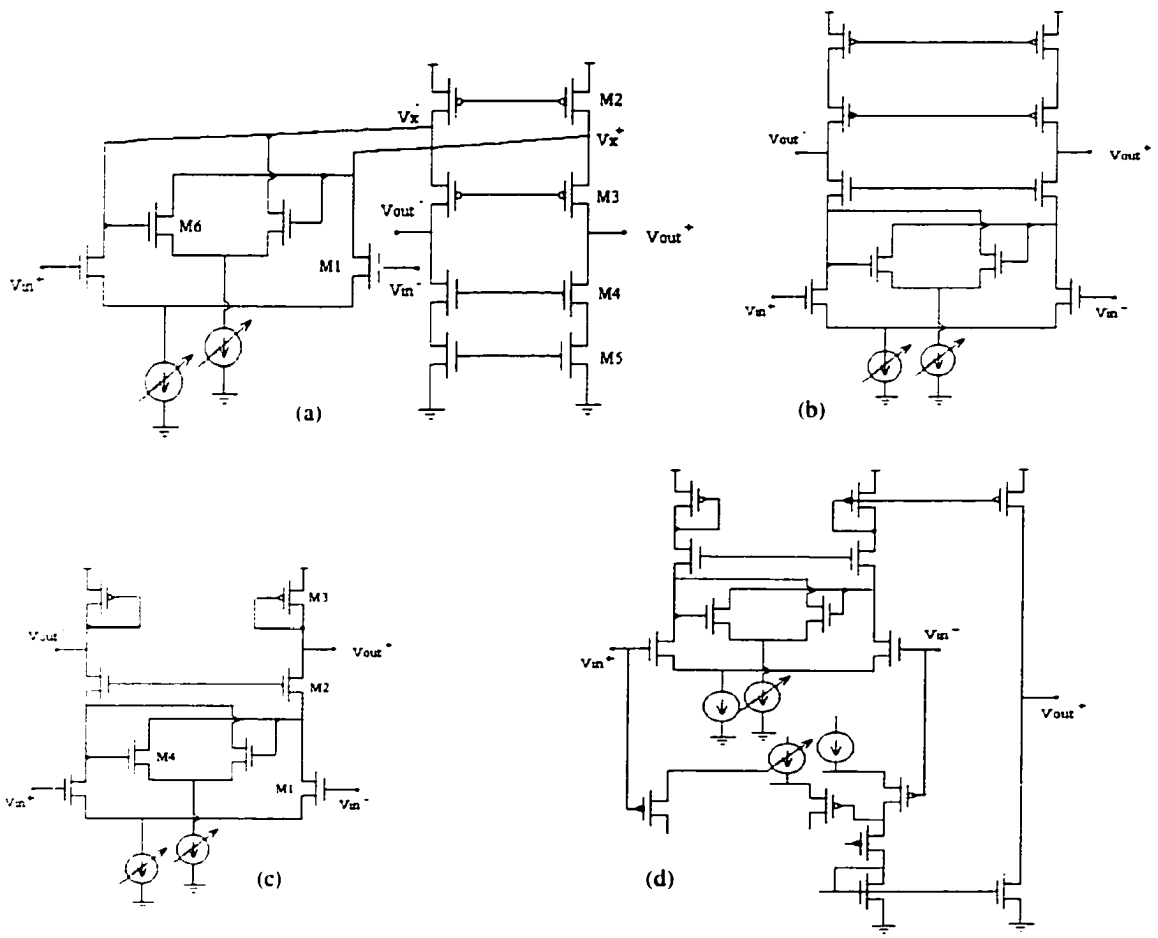



Fig. 4 Different implementations of the modified positive feedback technique for different popular amplifiers. (a) Folded Op-Amp with positive feedback. (b) Telescopic Op-Amp with positive feedback. (c) One sided cascode with positive feedback. (d) Rail-to-rail implementation with dual positive feedback.

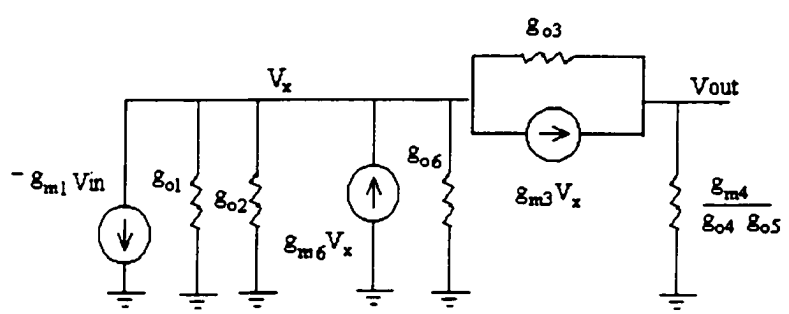



Fig. 5 Small signal model of one side of Op-Amp of Fig. 4.a

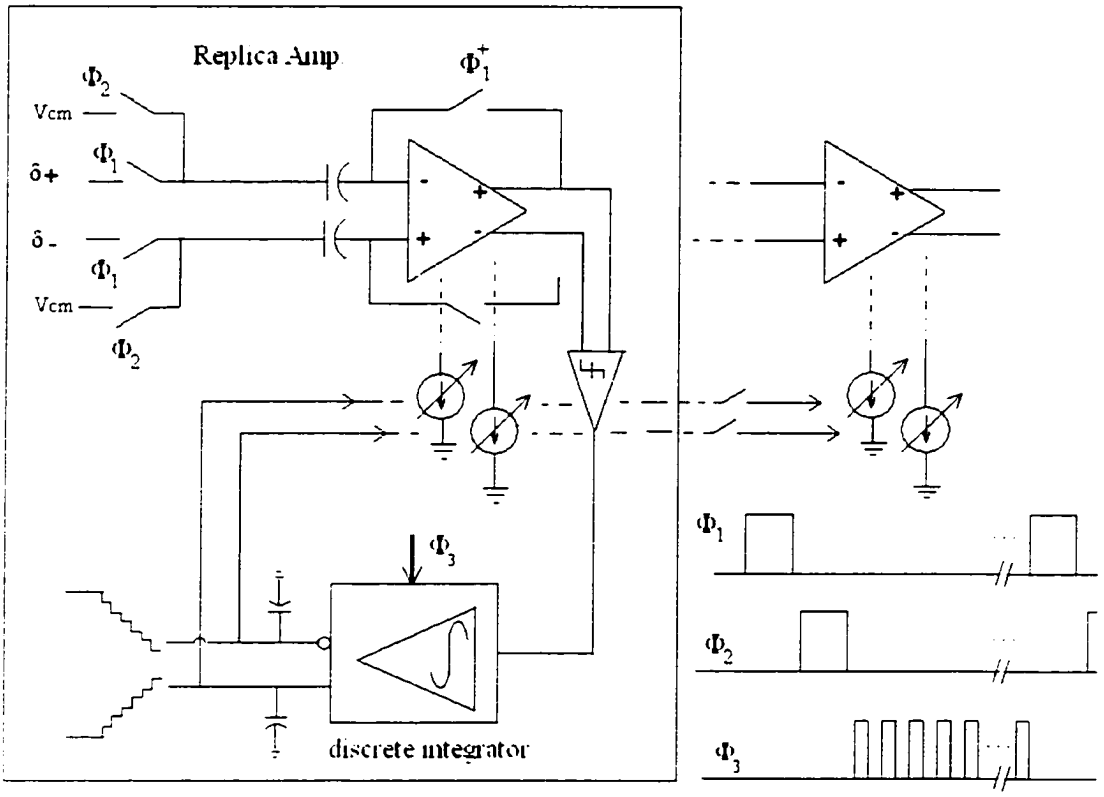



Fig. 6 Gain control mechanism using replica amplifier.

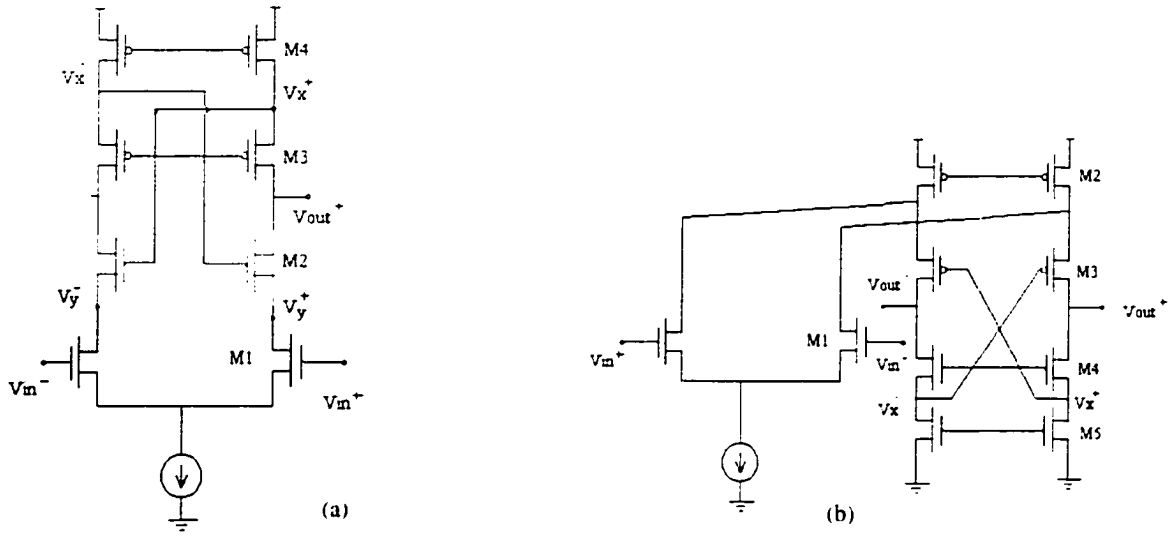



Fig. 7 Different possible implementations of the self tracking positive feedback technique. (a) Telescopic Op-Amp with positive feedback. (b) Folded Op-Amp with positive feedback.

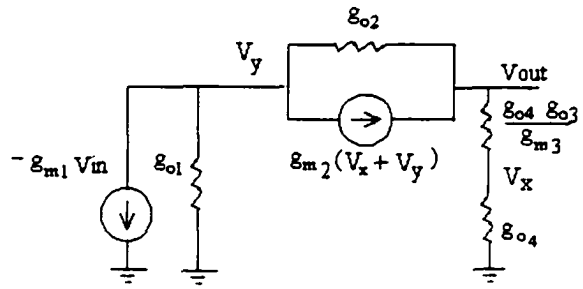



Fig. 8 Small signal model of one side of Amp. of Fig.7.a

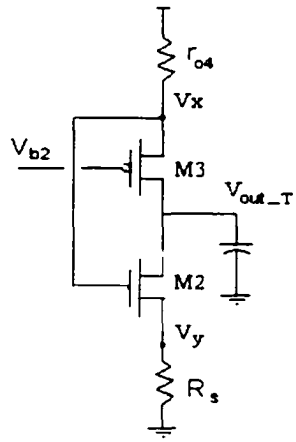



Fig. 9 Simplified common mode equivalent circuit for the amplifier of Fig. 7.a.

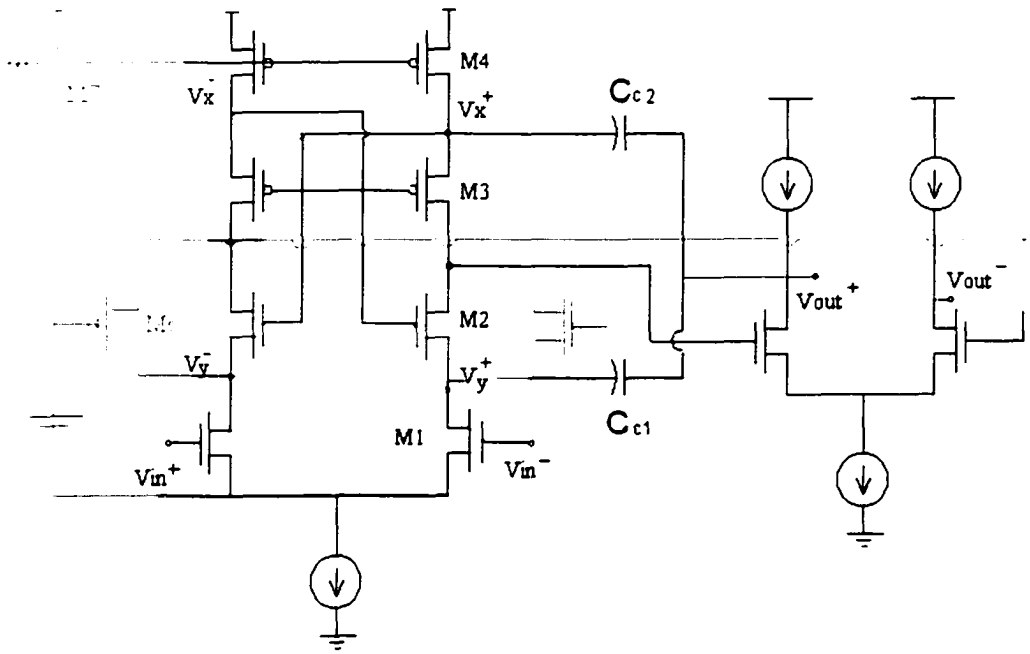



Fig. 10 Complete amplifier schematics.

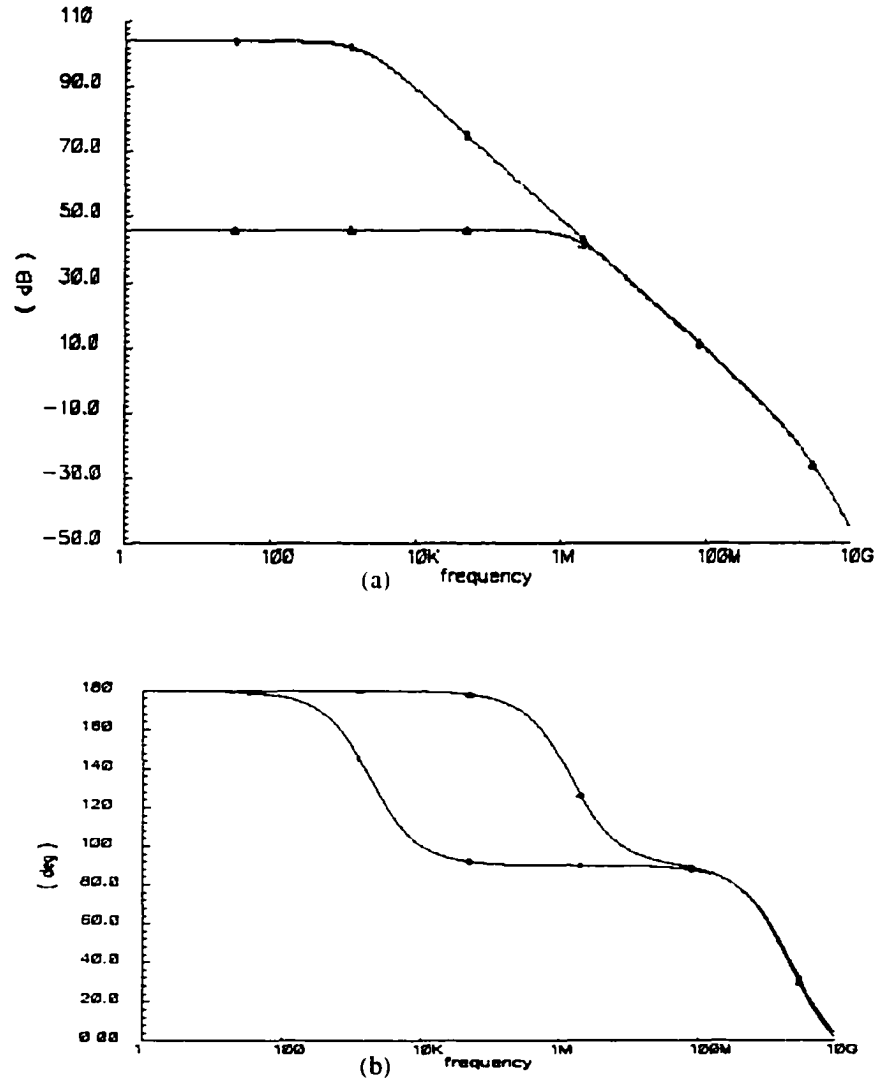



Fig. 11 AC characteristics of folded cascoded, with and without positive feedback. (a) Magnitude response. (b) Phase response.

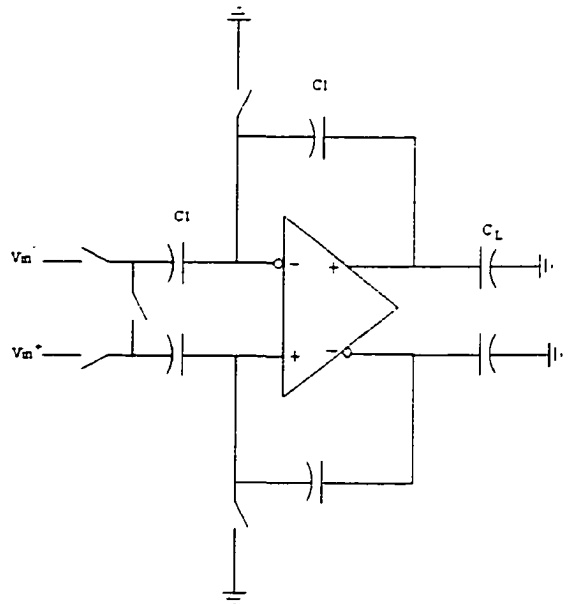
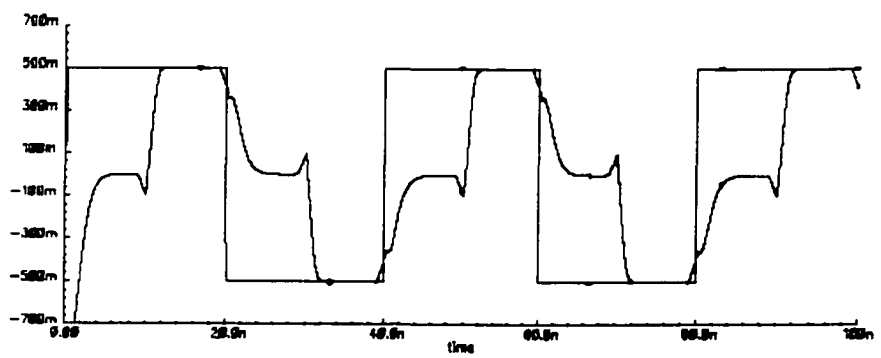
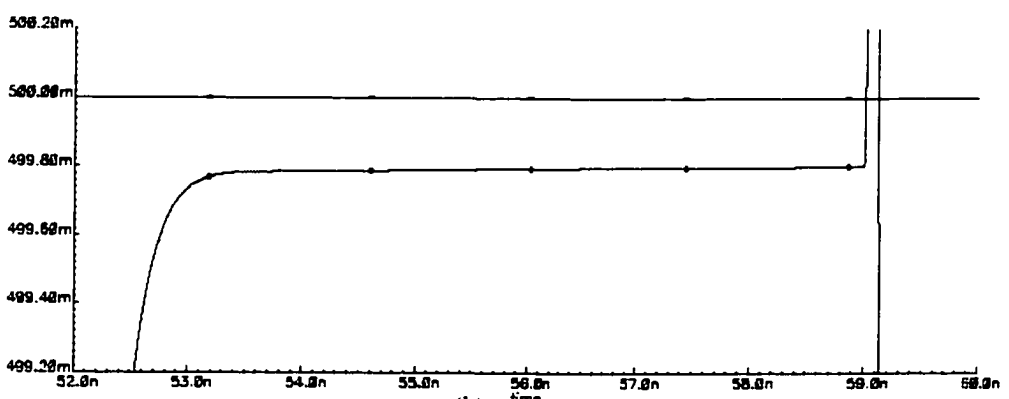



Figure 12 Amplifier of Figure 4.a in a sample and hold circuit.




(a)




(b)

Fig. 13 Sample and hold differential output, hold starts at 50ns. (a) multiple clock periods. (b) settling.

Table 1
Comparison of folded amplifier (Fig. 4.a) characteristics with/without positive feedback

| Folded cascoded | Positive feedback | Traditional |
|---|---|---|
| DC-gain | 103.7 dB | 46dB |
| Unity gain freq. | 278MHz | 288MHz |
| Load cap. | 500fF | 500fF |
| Phase margin | 82.5 degrees | 81.7 degrees |
| Total current | 0.8mA | 0.8mA |
| Supply voltage | 2.5V | 2.5V |

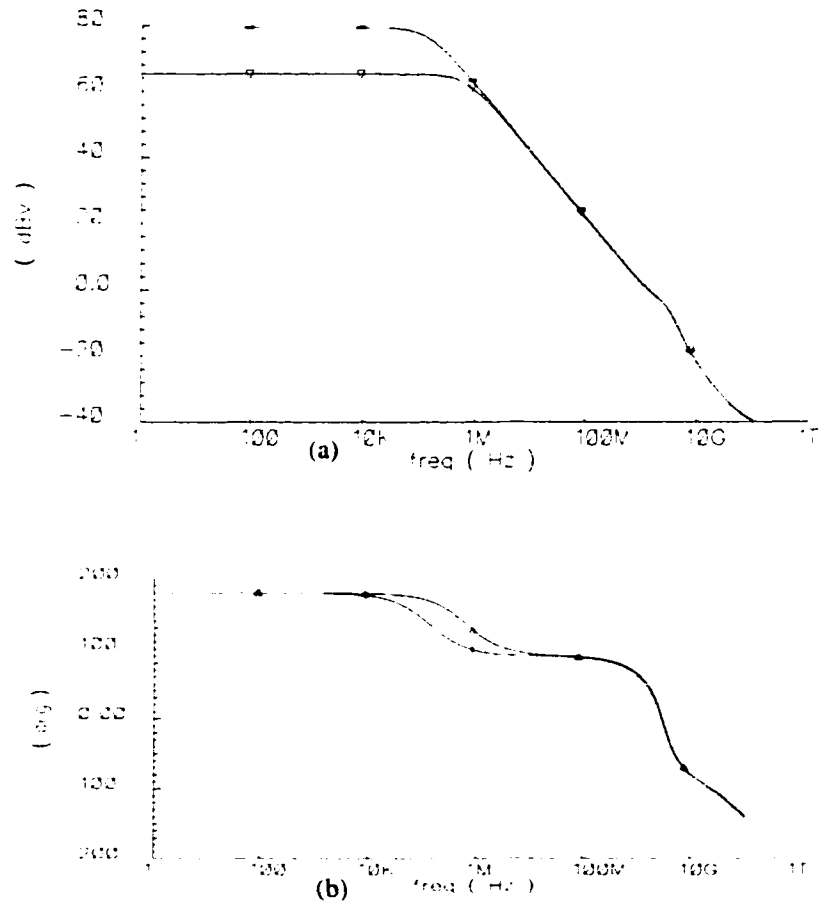



Fig. 14 AC characteristics of telescopic Op-Amp with and without positive feedback.
(a) Magnitude response. (b) Phase response.

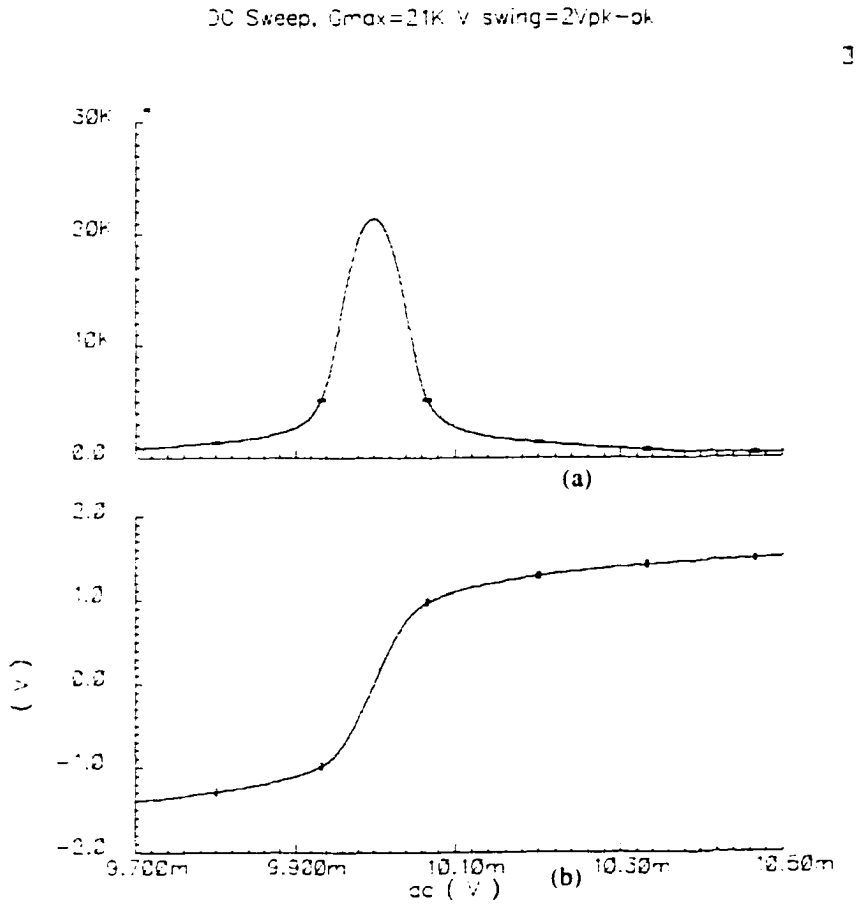



Fig. 15 DC sweep of amplifier in Fig. 10, 2.0$V_{p-p}$ swing. (a) gain. (b) input/output characteristics

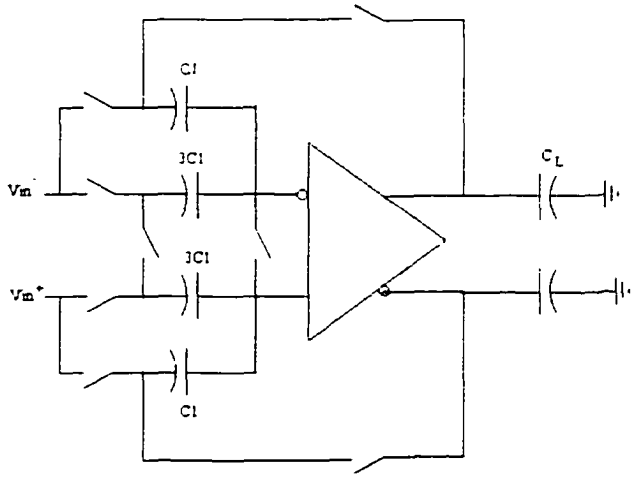



Fig. 16 Amplifier of Fig. 10. in a sample and hold circuit.

Table 2: Telescopic amplifier characteristics, Fig. 7a, with/without positive feedback

| Telescopic Amp | Positive feedback | Traditional |
|---|---|---|
| DC-gain | 80 dB | 64dB |
| Unity gain freq. | 1.218GHz | 1.234GHz |
| Load cap. | 1.0pF | 1.0pF |
| Phase margin | 63 degrees | 64 degrees |
| Total current | 8mA | 8mA |
| Supply voltage | 1.8V | 1.8V |

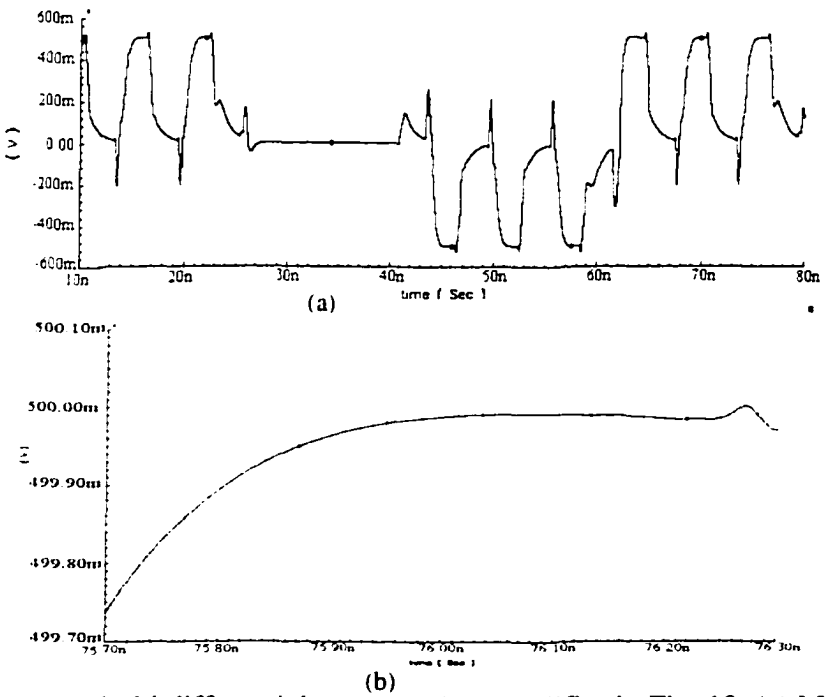



Fig. 17 Sample and hold differential output, using amplifier in Fig. 10. (a) Multiple clock cycles. (b) Settling.

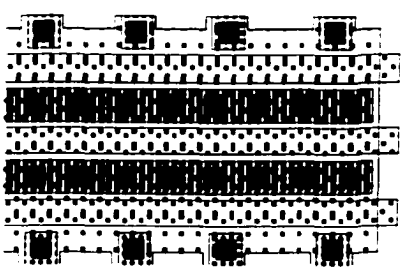


Fig. 18. Chopped-diffusion transistor-layout pattern.

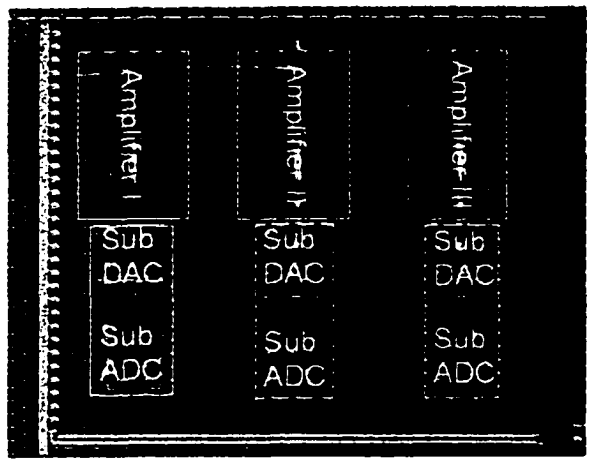



Fig. 20 Die photo of a 9-bit ADC implemented using the Op-Amp in Fig. 10.

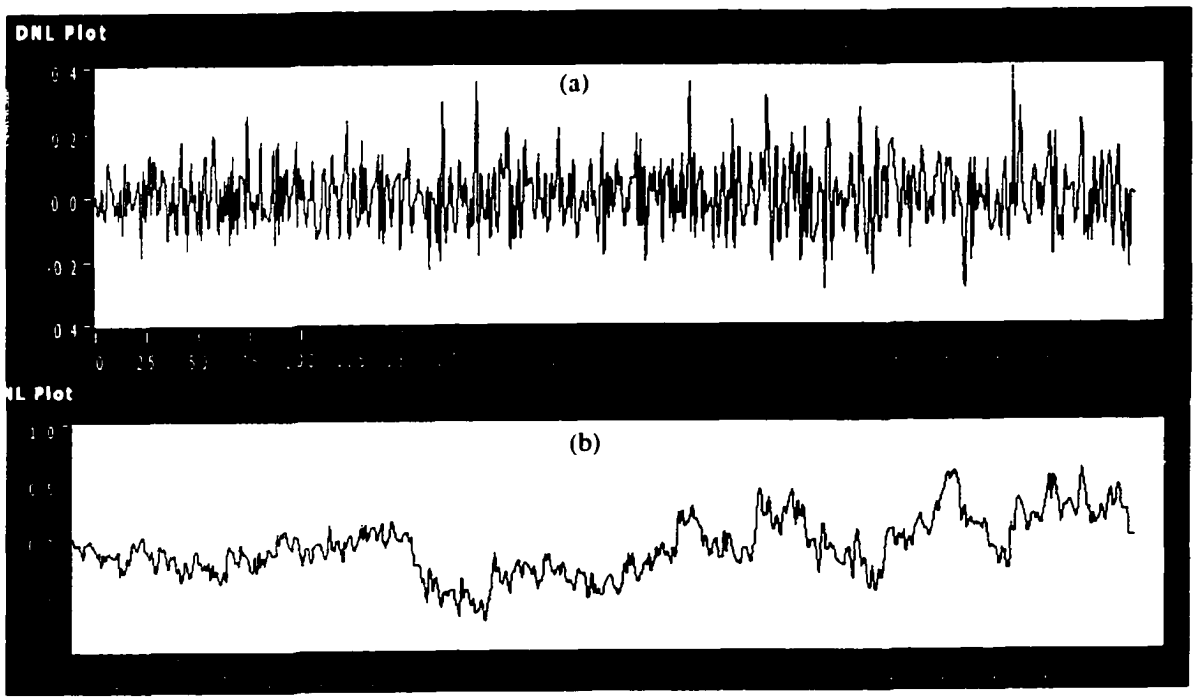



Fig. 21. Linearity test of the ADC at 82MS/s. (a) Measured DNL. (b) Measured INL.

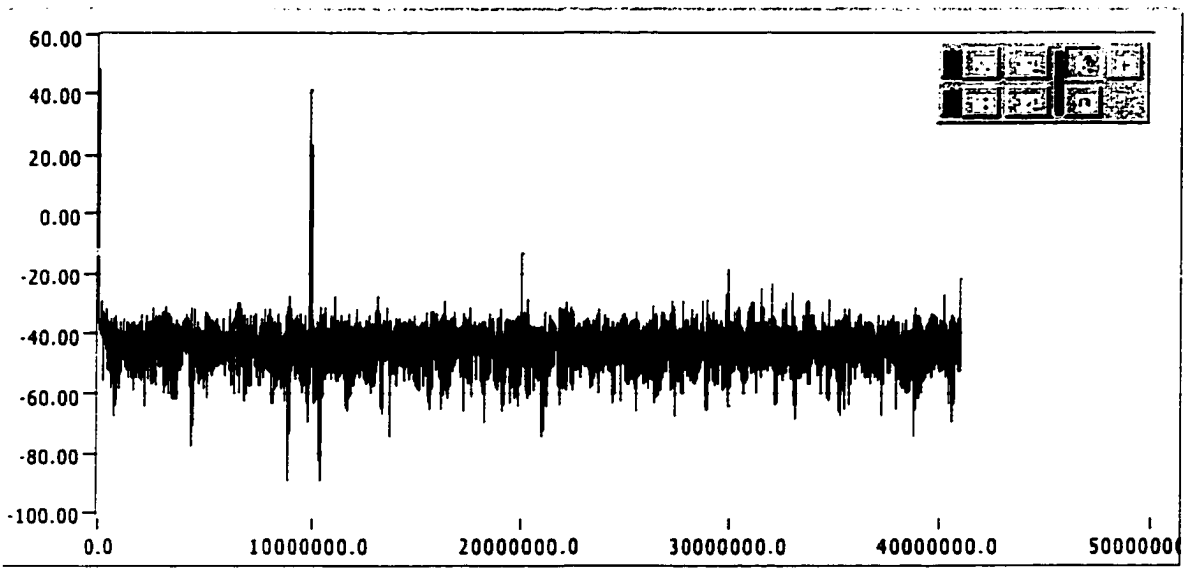



Fig.22 Output spectrum of the ADC output for 10MHz input and 82MHz sampling speed.

# GAIN AND BANDWIDTH BOOSTING TECHNIQUES FOR HIGH-SPEED OPERATIONAL AMPLIFIERS

A paper to be submitted to the IEEE Transactions on circuits and systems

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## Abstract

The finite gain and bandwidth of an operational amplifier are the main performance limitations for many applications. This paper describes two techniques to increase both amplifier bandwidth and DC-gain without changing the excess bias or the power dissipation. Implementations in continuous-time band-pass filters to demonstrate the excellent high frequency performance of the proposed architectures are described.

## 1. Introduction

Good linearity, accuracy, and high speed are the three most important properties of many analog circuits. A wide variety of integrated analog and mixed-signal systems have performance that is limited by the settling behavior of a CMOS operational amplifier (Op-Amp). These include continuous time and switched capacitor filters, algorithmic A/D converters, sigma-delta converters, sample and hold circuits, pipeline A/D converters [1], [2], [3], and others. The settling behavior of the Op-Amp determines the closed-loop accuracy and the speed that can be reached. Conventional wisdom suggests that fast settling requires a single pole settling behavior and a high gain-bandwidth-product [1, 2]. Short channel gate devices with low parasitic capacitance and small size devices will help increase the speed. High feedback accuracy generally requires a high DC gain. New submicron processes provide short channel, small sized devices that provide a fast response, but the low values of

intrinsic transistor gain inherent in these processes has made it increasingly difficult to build high DC-gain Op-Amps using previously known architectures.

A popular class of filters, Gm-C filters, is built with transconductance elements and capacitors [2]. Building accurate data converters and filters at very high frequencies present many problems [1, 2]. One major problem is the gain error in the data converter case, and the phase error of the integrator in the filter case [2], [4], [5]. Both amplifier gain error and integrator phase error are inversely proportional to the amplifier open loop DC gain. Concentrating on the filter application, the quality factor, Q, of the poles and zeros in the filter is highly sensitive to the phase of the integrator at the pole and zero frequencies [1]. To avoid errors in the filter characteristics, a sufficiently high amplifier DC-gain is required to build the desired integrator. This design problem has been addressed in several publications as in [1], [2]. Dynamic biasing of transconductance amplifiers has been proposed [4]. However, in dynamically biased amplifiers, and during the last settling period, transistors operate in the weak inversion region during the last part of the settling period which slows the settling. Moreover, dynamically biased amplifiers are applicable in the discrete time circuits only. Dynamically biased amplifiers have limited acceptance because of these disadvantages [1], [2]. Single-stage dynamically biased amplifiers do not provide sufficient gain for many applications, and the cascading of three or more stages is not practiced because of difficulty in compensating these structures [4]. Another approach for gain enhancement considered for filter applications is to use positive-feedback to enhance the amplifier DC-gain without limiting its high frequency performance. This approach was considered by Gray, Nuata and others [1,2]. However, most of the positive feedback implementations have suffered from three concerns. The first is the strong dependence of amplifier gain on precise

transistors parameter matching [1,3]. The second is the strong gain sensitivity to the input/output signal swings. The third is the possibility of unstable operation. The high gain sensitivity comes from the fact that the positive feedback in reported structures is taken from the output nodes that exhibit wide swings. Because of amplifier none linearity, the DC-gain of the amplifier will drop dramatically as the output node swings up or down. In spite of the previous concerns, the positive feedback technique shows good potential for building fast settling amplifiers with high DC gain that are suitable for low voltage applications. Besides the possibilities of enhancing existing amplifier DC gain, we will discuss methods of enhancing amplifier transconductance. This will lead to faster operation.

In this paper we will discuss two methods that can be used to build amplifiers that have a combination of high DC-gain and enhanced transconductance without increasing the power dissipation and without changing the excess bias at the input nodes. The amplifiers discussed will be applicable to continuous-time and to switched-capacitor systems.

## 2- Transconductance and DC-Gain Enhancement Techniques

Amplifier transconductance, $G_m$, is generally a function of the transconductance of transistors at the input, $g_{mi}$. The transconductance of the input transistors can be increased by increasing the biasing current or by increasing the sizes of the input transistors [5]. Since $g_{mi}$ can be expressed as

$$g_{mi} = \sqrt{\frac{\mu C_{ox} W}{L} \cdot 2 \cdot I_{ds}} \tag{1}$$

Increasing $I_{ds}$ linearly will cause a quadratic increase in power dissipation [5]. Either of these two ideas will result in tradeoffs. Increasing W/L ratio will increase the parasitic capacitances

at the input nodes, and increasing W/L without increasing the biasing current will result in limiting the swings at the input of the amplifier.

Here we are going to present two other methods that can be used to enhance the overall amplifier transconductance while increasing the DC gain at the same time. Both techniques depend on using the transistors that provide output impedance enhancement as amplifying transistors too. The positive feedback technique will be used to enhance the DC gain with minimal additional circuitry. To avoid the concerns about positive feedback mentioned above, we will consider implementations where the parameters of some of the devices in the positive feedback path will be either controllable or have self-adjusting property. Such implementations will relax the constraints on matching. The stability concern is not really a problem because when the Op-Amps are used in negative feedback applications, the closed loop poles will be far in the left half plane irrespective of wether the open-loop amplifier has a left half plane or right half plane poles [1]. It is practical to guarantee that the dominant pole of the overall system is in the left half plane even though the open-loop amplifier has a right half plan (RHP) pole [1,7]. For the rest of this work transconductance and gain formulas are derived for differential input differential output signal.

The first technique, which is applicable to amplifiers depends on the traditional practice of connecting the active load transistors to the input signal rather than to a fixed biasing voltage. This approach may require a DC shift in the connection to the active load transistors to make the input voltage proper to drive the active load transistor. A second modification of the traditional approach is to eliminate the requirement of a common feedback circuit (CMFB) to enhance the supply rejection ratio. To make the biasing of transistors more robust, we will use some resistive connection to the supply. This resistive connection

will provide the positive-feedback. This technique allows us to increase the amplifier transconductance, $G_m$, without increasing the power dissipation, the transistor sizes, or without reducing the excess bias on the input transistors.

Consider the amplifier shown in Fig. 2a that has a short-circuit transconductance, $G_m$. The amplifier shown in Fig. 2b has a differential transconductance, $G_m$, given by

$$G_m=-(g_{m1}+g_{m2}) \tag{2}$$

that is twice the $G_m$ of amplifier in Fig. 2a. for the same power dissipation, the same excess bias on $M_1$ and $M_2$, of course the if the length of $M_1$ and $M_2$ are the same, this increase in Gm is obtained at the expense of an increase of input capacitance by a factor 4and a reduction in input common mode range. Since the amplifier gain bandwidth product and the DC gain are proportional to $G_m$, and since the output conductance does not change, the amplifier in Fig. 2.b has also twice the DC-gain and twice the gain bandwidth product as the amplifier in Fig. 2.a. Transistor M2 sense as a biasing transistor in Fig. 2a, but becomes an amplifying device in the circuit of Fig. 2b. If excess bias of transistors $M_1$ and $M_2$ are the same a problem that appears in the amplifiers in Fig. 2 is the need for a CMFB circuit that should be at least as fast as the amplifier itself [5]. This requires a lot of power dissipation in the CMFB circuit. Moreover, transistor M2 in Fig. 2b has an excess bias is directly affected by the supply voltage variations, thus the amplifier will exhibit poor supply rejection performance.

Modifications on Fig. 2b are shown in Fig. 3. None of these amplifiers need a CMFB circuit. Transistor M3 in Fig. 3a and Fig. 3c operates in saturation region, while in Fig. 3b and Fig. 3d in the ohmic region. The amplifiers in Fig. 3.a,c have limited output swings and limited common mode input swings compared to the amplifiers in Fig. 3b,d. The amplifiers in Fig. 3a,c have a transconductance equal to;

$$G_m = -\left( g_{m1} + \frac{g_{m2} \cdot (\pm g_{m3})}{g_{m2} \pm g_{m3} + g_{o2} + g_{o3}} \right) \tag{3}$$

Minus sign with $g_{m3}$ term is applicable for the positive feedback case. Amplifiers in Fig. 3b,d have a transconductance equal to

$$G_m = -\left( g_{m1} + \frac{g_{m2} g_{o3}^{\cdot}}{g_{m2} + g_{o2} + g_{o3}^{\cdot}} \right) \approx -\left( g_{m1} + \frac{g_{m2}}{2} \right) \tag{4}$$

where $g_{o3}^{\cdot}$ is the output conductance of the PMOS transistor $M_3$ which operates in the ohmic region. $g_{o3}^{\cdot}$ is close in value to $g_{m2}$. Amplifiers shown in Fig. 3c,d have the positive feedback property. The amplifier shown in Fig. 3.d has a very high unity gain frequency as will be shown in the next section. Amplifiers in Fig. 3.a,c have a differential DC gain of the form;

$$A_V = -\frac{g_{m2}\left[g_{m1} g_{m2} + g_{m1} g_{m3} + g_{m2} g_{m3}\right]}{\left[g_{m2} + g_{m3}\right]\left[g_{m2} g_{o1} \pm g_{m3} g_{o2}\right]} \tag{5}$$

The negative sign in the denominator is applicable when the positive feedback exists as in Fig. 3.c. On the other hand small signal analysis shows that the amplifiers in Fig 3.b,d have a DC gain of the form;

$$A_V = -\frac{g_{m1}\left(g_{m2} + g_{o2} + g_{o3}^{\cdot}\right) + g_{m2} g_{o3}^{\cdot}}{\left(g_{m2} + g_{o2} + g_{o3}^{\cdot}\right)\left(g_{o1} + g_{o2}\right) \pm \left(g_{m2} + g_{o2}\right)\left(g_{o2} + g_{m3}^{\cdot}\right)} \tag{6}$$

Again $g_{o3}^{\cdot}$ and $g_{m3}^{\cdot}$ are the parameters of the transistor $M_3$ in the ohmic region. Negative sign in the denominator of the gain formula is applicable when positive feedback exists, that is in Fig. 3.d. The amplifier of Figure 3.d can show a DC gain as high as 60dB which makes it suitable for filter applications where very high speed operation with low power dissipation are the key features, also it is very useful as a pre-amplifier for fast voltage comparators. Because the denominator of Eq. (6) includes different types of parameters, it is very hard to match them together over temperature and process variations. The drawback of this

technique is the increase of the amplifier input capacitance which reduces the effective speed enhancement. However some tricks can be used to reduce amplifier input capacitance. Those tricks include using extra cross coupled capacitors between the input nodes and output nodes. This will make the capacitors at the input look as negative capacitors. Other tricks are biasing tricks like reducing the transistor size (W/L) ratio by increasing the excess bias for a fixed quiescent current. Finally, in the above expressions, the body effect has been neglected for simplicity of expressions. Although it affects the gain expressions nominally, the positive feedback inherently compensates for the body effects as well.

The second technique is applicable to amplifiers with one level of cascoding. The basic idea is implemented in two steps. As a reminder traditional cascoded architectures have two cascoded transistors connected to the output node, traditionally only one side of the cascode is in the signal path. For maximum utilization of the consumed power, we will excite both sides of the cascode. The second step is to drive the transistor in the cascode with a signal as will as shown in Fig. 4. The voltage $K_1 \cdot V_{in}$ at the gate of cascode transistor $M_1$ can be a feedback from another cascode node. In this example shown in Fig. 4 with assumptions shown below, this amplifier has a transconductance of the form;

$$G_m = -\frac{g_{m1} g_R K1 + (g_{m1} + g_{o1}) K2}{g_{m1} + g_R + g_{o1}} \approx -2g_{m1} \quad where \qquad K2 \propto g_{min}; \quad K1 \propto \frac{g_{min}}{g_R} \tag{7}$$

So employing the cascode transistor as an amplifying one may double the transconductance under the assumptions mentioned in detail in Eq. (7). The realization of this two step concept, positive feedback signals were also taken from the cascode nodes to reduce the gain sensitivity to the output signal swing. Moreover some devices involved in the positive feedback loop will have controllable parameters as will be shown next. Examples of the

possible implementations of this technique on folded and telescopic cascode amplifiers are shown in Fig. 5.a,b. For the rest of this paper we will concentrate on the amplifier shown in Fig. 5a, the amplifier shown in Fig. 5.b inherits the same properties

Fig. 6 shows one side of the amplifier of Fig. 5a from the small signal perspective. To implement the first step we were forced to split the input differential pair into two pairs. A small signal analysis of Fig. 6 shows that the proposed amplifier has a transconductance, $G_m$, of the form;

$$G_m = -\frac{g_{m6}g_{m3}(g_{o1}+g_{o2}+g_{o4})+g_{m6}g_{m4}(g_{o1}+g_{o2}+g_{o3})+g_{m1}g_{m3}(g_{o4}+g_{o5}+g_{o6})+g_{m1}g_{m4}(g_{o3}+g_{o5}+g_{o6})}{g_{m3}(g_{o4}+g_{o5}+g_{o6})+g_{m4}(g_{o1}+g_{o2}+g_{o3})} \quad (8)$$

This equation shows that amplifier $G_m$ is approximately equal to $(2g_{m1}+2g_{m6})$ if we assume that, $g_{o1}\approx g_{o6}$, and $g_{o3}\approx g_{o4}$. The regular folded cascode has a $G_m$ value of $g_{m1}^*$. An initial observation would suggest that for the amplifier of Fig. 5a, the transconductance should be around four times that of regular folded amplifier because we are using both sides of the cascode to drive the signal, and we are making the transistors in the cascode amplifying ones, $G_m \approx 4g_{m1}^*$. But note that there is a difference in the biasing currents between the suggested implementation in Fig. 5a and the traditional folded case if we are consuming the same power. In reality gm1 or gm6 of Fig. 5a has approximately a value of (2/3) of $g_{m1}^*$ of the traditional case under the constant power assumption depicted in Fig. 7. A comparison between the two architectures transconductances shows that we have an enhancement factor of (8/3). We should not neglect the increase in amplifiers input capacitance which is increased by a factor of 1 to 4 depending on the implementation, and which will reduce the effective increase in speed. However, again some tricks can be used to reduce the input capacitance back to its original value as mentioned earlier. Estimating the DC-gain, $A_v$, of Fig. 6 results in;

$$A_v = -\frac{(g_{m3}+g_{m4})[g_{m6}(g_{o1}+g_{o2})+g_{m1}(g_{o5}+g_{o6})]+(g_{m1}+g_{m6})(g_{m3}g_{o4}+g_{m4}g_{o3})}{(g_{o1}+g_{o2}-g_{o5}-g_{o6})(g_{m3}g_{o4}-g_{m4}g_{o3})} \quad (9)$$

The denominator of Equation (9) shows that the proposed amplifier exhibits a positive feedback property and shows potential for dramatic gain enhancement.

In our design we concentrated on getting our high gain by making the term, $g_{o5}+g_{o6}$, very close to the term, $g_{o1}+g_{o2}$. Looking back at Fig. 5a we see that by controlling the current source we are controlling both $g_{o5}$ and $g_{o6}$. This allows us to control the amplifier gain, and not to be totally dependent on the transistor matching issue. Biasing the amplifiers shown in Fig. 5 requires a replica biasing scheme if we want to make sure that a very high DC-gain is to be maintained always with very small variability over temperature and process corners. However, since $g_{oi}$ depends on the biasing current, and since $M_1$ and $M_5$ are NMOS transistors while $M_2$ and $M_6$ are PMOS transistors, then if we make the amplifier gain dependent on the term $(g_{o1}+g_{o2}-g_{o5}-g_{o6})$, and if we have good CMFB circuits, then the amplifier can maintain the high DC gain if designed carefully even without gain control circuit. Simulations show that without a gain control, the amplifier can maintain high DC gain with a maximum variation of less than 14dB across process and temperature corners for a nominal gain of 107dB. As a reminder, the main drawback of the amplifier in Fig. 5a is the increased input capacitance of the amplifier. The output parasitic capacitance of this proposed amplifier is lower than that of the regular folded cascode by a factor of one third approximately, due to smaller transistor sizes because of the lower biasing currents flowing through transistors $M_3$, and $M_4$. In the next section we will describe simulation results of the proposed amplifiers. We will also show an application of the proposed amplifiers shown in Fig. 3d, and Fig. 5a in a continuous-time band-pass filter.

## 3. Simulation Results

The amplifier shown in Fig. 3d has been simulated using the TSMC 0.25u process. The amplifier has a total current of 340uA, a load capacitance of 500fF, and power supply of 2.5 Volts. Simulations show that the amplifier can achieve a DC gain of 66dB and a unity gain frequency of 842MHz with a phase margin of 87 degrees. Results for AC analysis are shown in Fig. 8. For simplicity the phase shown for the AC analysis is shifted up by 180 degrees so the phase margin can be read directly from the figure. Parasitic elements are included in all the simulations in this section and all simulation results are for differential output signals.

The modified folded amplifier of the second technique with the positive feed-back was simulated using CMOS TSMC 0.25u process. The amplifier consumes a total current of 1.2mA driving a capacitive load of 500fF and biased by a power supply of 2.5V. The simulation shows that the amplifier has a DC gain as high as 107.3dB with a unity gain frequency of 805MHz. A comparison between the modified and the traditional folded cascode is shown in Table 1 where both amplifiers have approximately the same power dissipation, the same excess bias on the similar transistors, and the same load capacitance. The table shows that for the same conditions we were able to enhance both the unity gain frequency from 433.5MHz to 805MHz and the DC-gain from 47.23dB to 107.3dB for the same load and approximately for the same phase margin. Results are shown in Fig. 9. Again the phase response in Fig. 9b is shifted up by 180 degrees to show the phase margin directly from the figure. The proposed amplifier architectures have been implemented in a continuous time $4^{th}$ order Butterworth band-pass filter. The filter is constructed by cascading two Gm-C biquads, as shown in Fig. 10. The only difference between the two biquads is the value of the

damping transconductor ($g_{m2}$). The filter has a transfer function, center frequency, and bandwidth given by the following relationships [8].

$$\frac{V_o}{V_i} = \frac{g_{m1} sC_2}{s^2 C_1 C_2 + sC_2 g_{m2} + g_{m1}^2} = \frac{\frac{g_{m1} s}{C_1}}{s^2 + s\frac{g_{m2}}{C_1} + \frac{g_{m1}^2}{C_1 C_2}} \tag{10}$$

$$\omega_o = \frac{g_{m1}}{\sqrt{C_1 C_2}} \tag{11}$$

$$BW = \frac{g_{m2}}{C_1} \tag{12}$$

The transconductance amplifier of Fig. 3d implemented in the filter consumes a total current of 4mA. Capacitors have sizes, $C_1$=1.2pF, $C_2$=1pF. The simulated OTA has its open loop pole in the right half plane, still the closed loop operation is stable as shown. This point of operation for the OTA has been selected simply because the positive feedback in OTA of Fig. 3d is not controllable, and this point of operation has shown minimum amplifier characteristics variation, sensitivity, over temperature and process corners. Simulation results are shown in Fig. 11 for the typical corner. As shown in Fig. 11a. Simulation results show that the filter has a center frequency of 1.047GHz, and a bandwidth of 380MHz. Transient simulation shows that the filter can achieve a 360m$V_{p\text{-}p}$ output swing. Discrete fourier analysis shows that at the maximum swing for an input at 1.04GHz, the total harmonic distortion is –30dB. The same filter architecture is implemented using the OTA shown in Fig. 4a with a total current of 4.0mA. Capacitors have sizes, $C_1$=1.2pF, $C_2$=0.6pF. Simulation results are shown in Fig. 10. Simulation results show that, the filter has a center frequency of 1.216GHz, and a bandwidth of 250MHz. Transient simulation, shows that the filter can

achieve a $300mV_{p-p}$ output swing. Discrete fourier analysis shows that at the maximum swing for an input at 1.216GHz the total harmonic distortion is –32.6dB.

## 4. Conclusions

Two techniques to enhance amplifier transconductance in addition to Positive-feedback have been proposed to build high speed and very high DC-gain amplifiers. In this work we were able to verify that we can enhance the transconductance of some well known amplifiers without increasing the power dissipation or limiting the input/output swings. The first technique is applicable to non cacoded structures. The second technique is applicable to cascoded structures with at least one level of cascoding. In this case, the positive feedback is controllable and has low sensitivity to output signal swings. The extra price paid was the increase of the amplifier input-capacitance.

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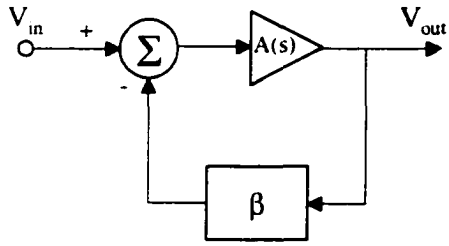



Fig. 1 General amplifier in a closed loop circuit.

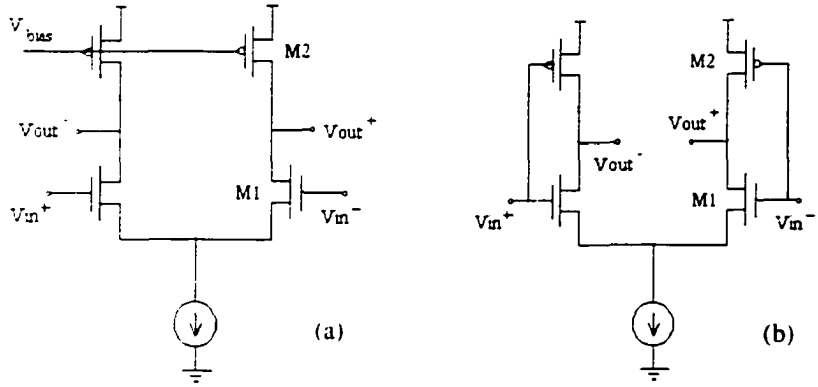



Fig. 2 Speed enhancement method. (a) Basic amplifier. (b) Enhanced Gm amplifier.

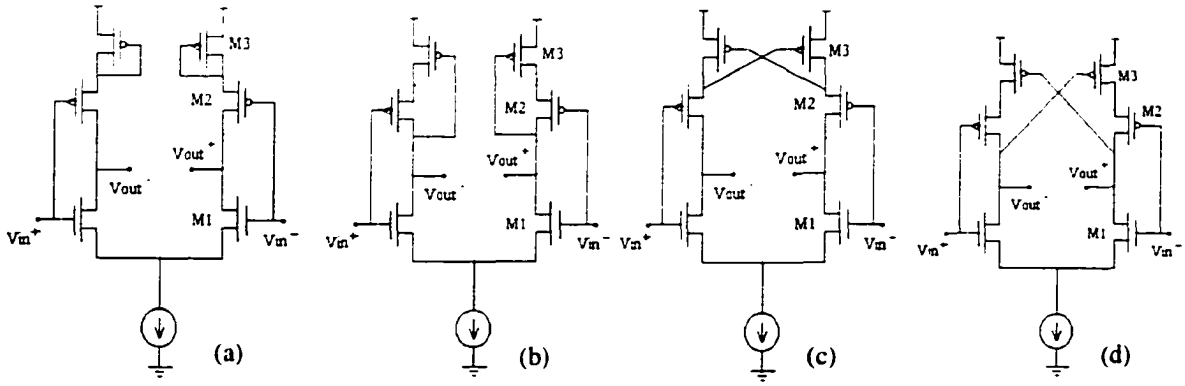



Fig. 3 Modifications on Fig. 2b. where no CMFB circuit required (a) $G_m$ enhanced, low swing. (b) $G_m$ enhanced high swing. (c) low swing with positive feedback. (d) High swing with positive feedback.

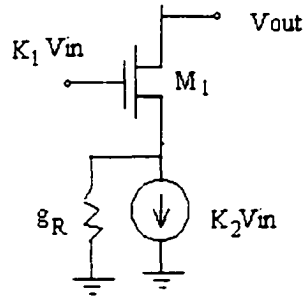



Fig. 4 Proposed second step to enhance amplifier's transconductance.

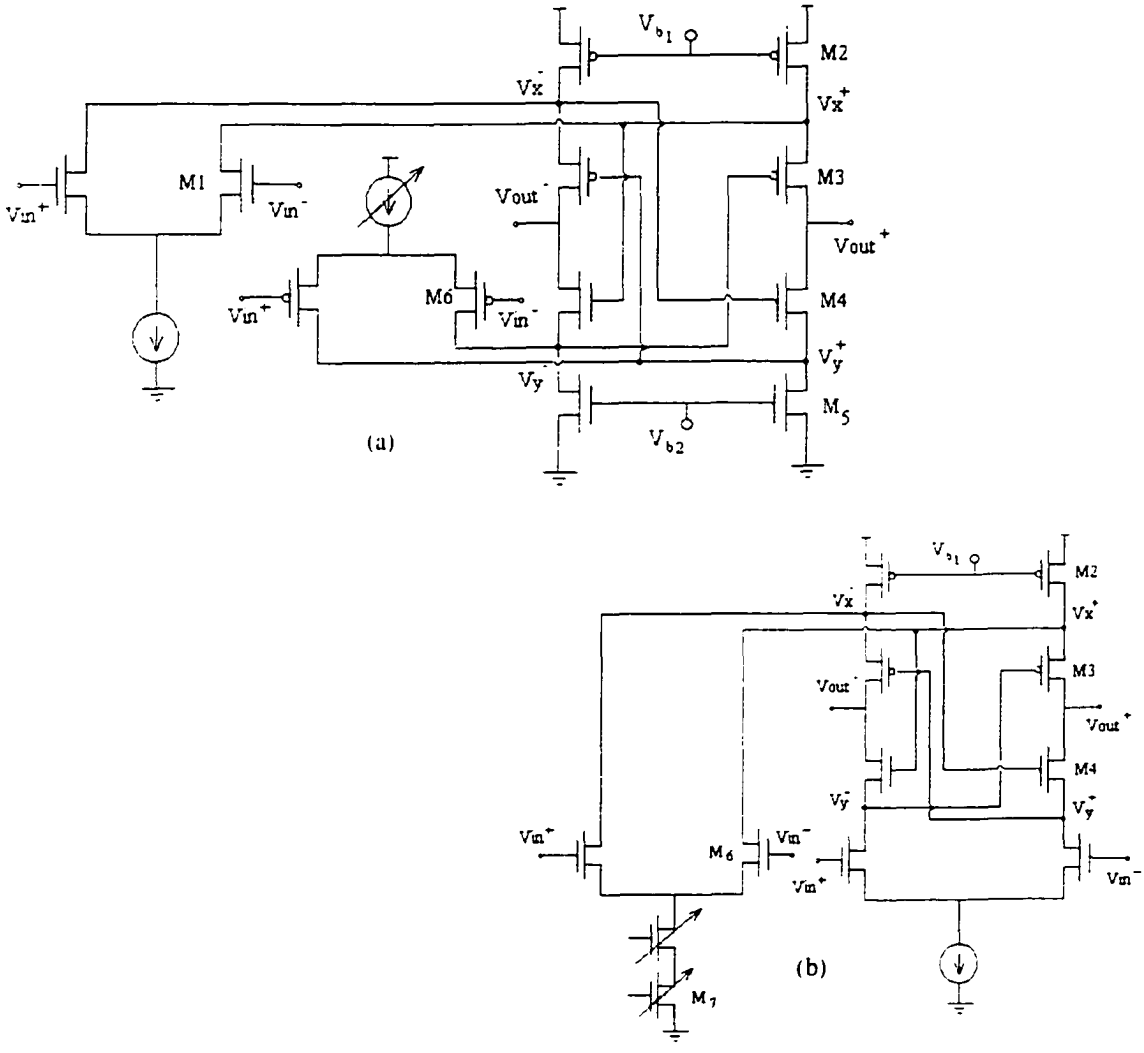



Fig. 5. $G_m$ enhancement technique with positive-feedback applied. (a) Folded cascode. (b) Telescopic cascode.

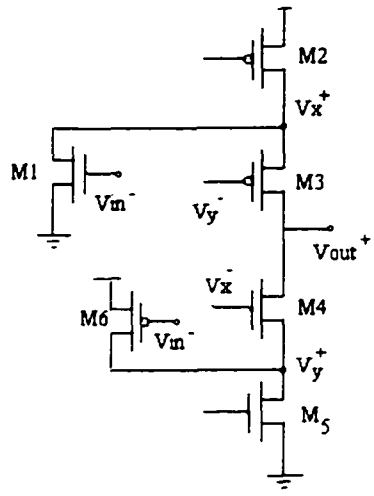



Fig. 6. One side of amplifier in Figure 5.a from small signal perspective.

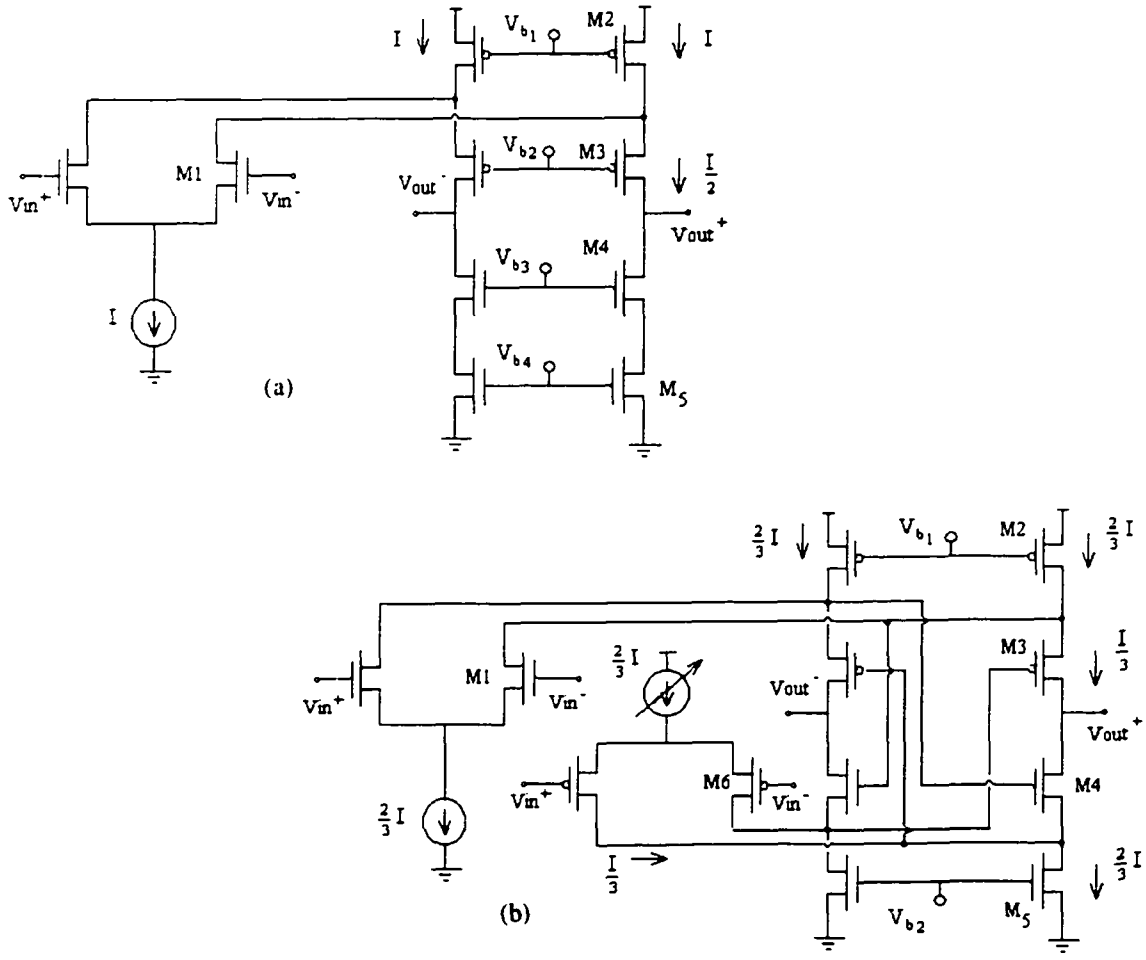



Fig. 7 Biasing currents, constant power. (a) Regular folded. (b) Modified folded.

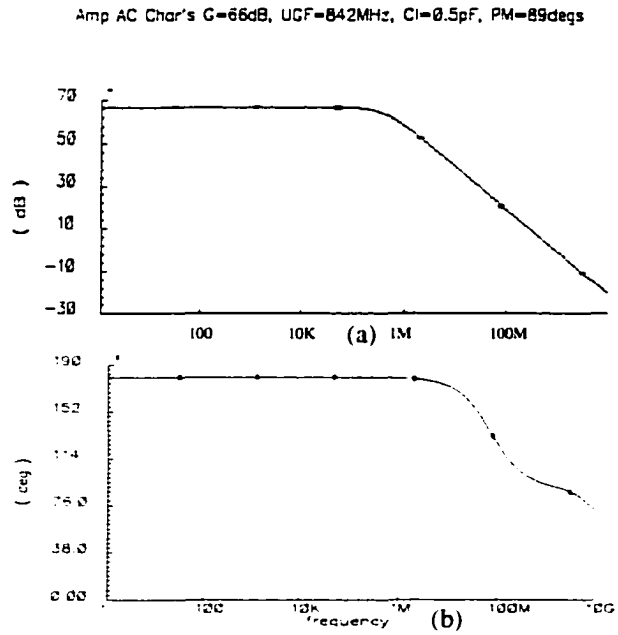



Fig. 8 AC analysis of the amplifier in Fig. 3d. (a) Magnitude response. (b) Phase response.

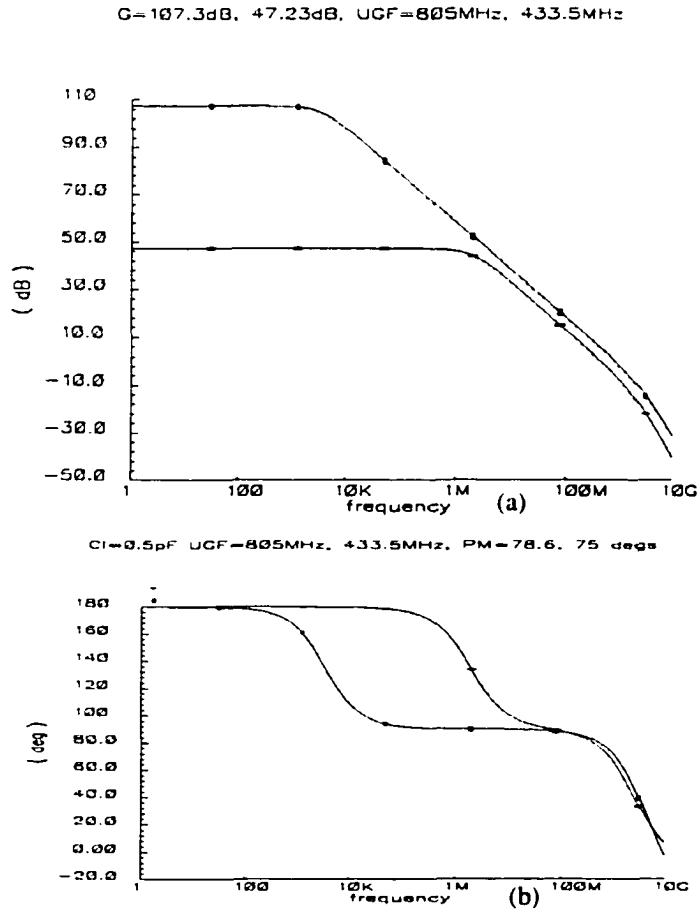
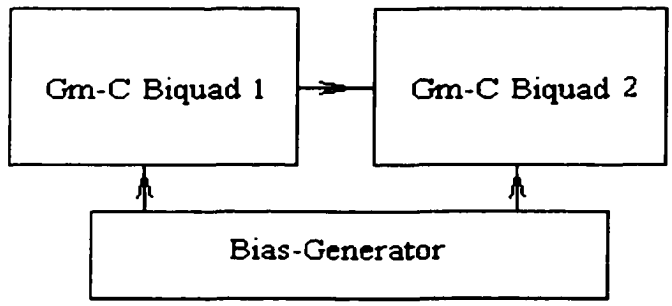


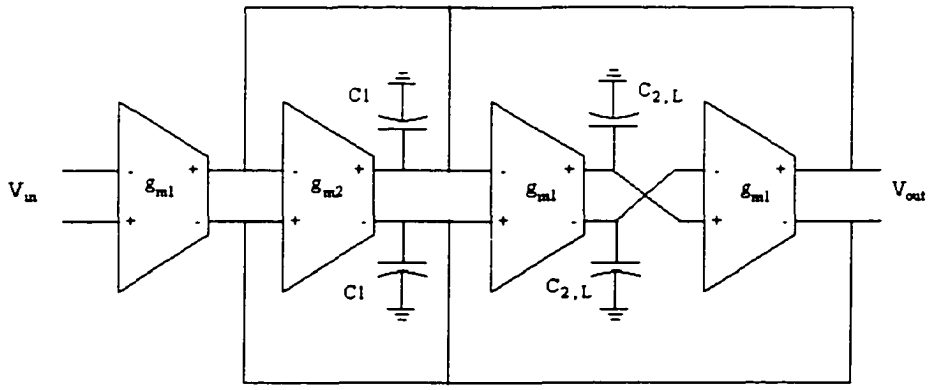

Fig. 9 AC response of the folded and the enhanced folded cascode. (a) Magnitude. (b) Phase.

Table1
Comparison of Amplifier Characteristics w/wo $G_m$ enhancement Tech.

| Folded cascoded | Gm-Enhanced | Traditional |
|---|---|---|
| DC-gain | 107.3 dB | 47.23dB |
| Unity gain freq. | 805MHz | 433.5MHz |
| Load cap. | 500fF | 500fF |
| Phase margin | 75 degrees | 78.6 degrees |
| Total current | 1.2mA | 1.2mA |
| Supply voltage | 2.5V | 2.5V |




(a)




(b)

Fig. 10 The 4th order Band-pass filter. (a) Filter block diagram. (b) biquad block diagram.

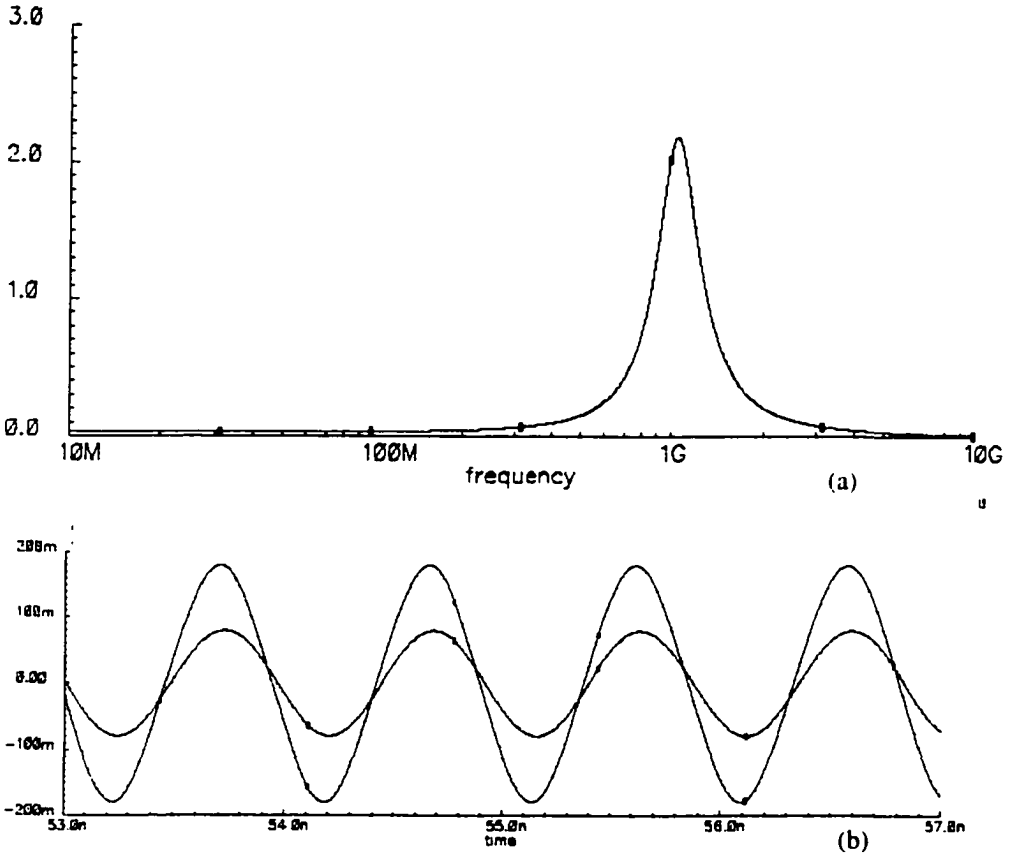



Fig. 11 Filter characteristics using OTA of Fig. 3d (a) Magnitude response. (b) Transient input and output waveforms at 1.047GHz

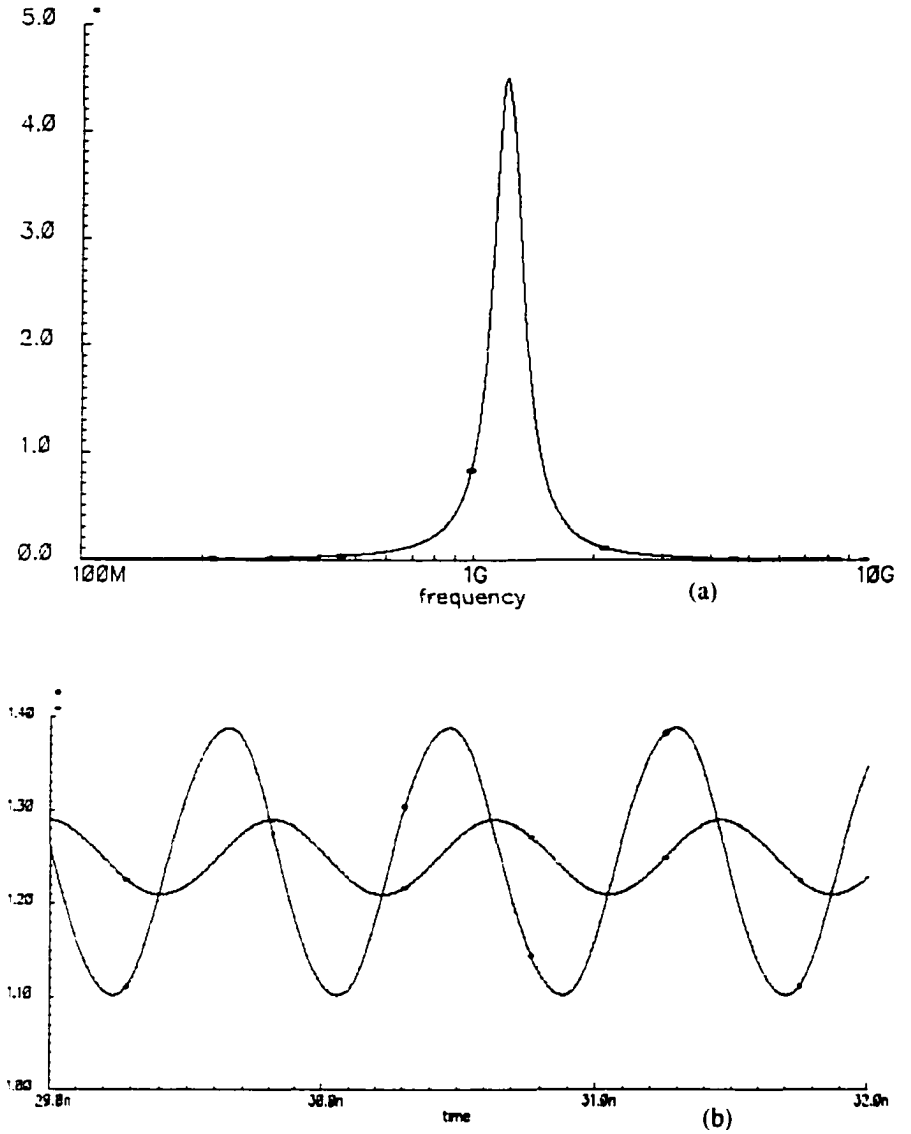



Fig. 12 Filter Characteristics using OTA of Fig. 5.a. (a) Magnitude response. (b) Transient Input and output waveforms at 1.216GHz

# A 9B 165MS/S 1.8V PIPELINED ADC WITH ALL DIGITAL TRANSISTORS AMPLIFIER

A paper to be submitted to the IEEE Journal of Solid State Circuits

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## Abstract

A 9bit, 1.8V, 165MS/s pipelined ADC was built in a 0.21μ CMOS digital process. The interstage amplifier in this converter was built using all digital transistors. To get sufficient gain with digital transistors, a self-adjusting positive feedback operational amplifier that shows low sensitivity to output swing was used. The ADC consumed a total power of 90mW when operated at full speed.

## 1. Introduction

There is an increasing demand for high-speed signal processing applications such as HDTVs, digital camcorders, and portable data communications [1]. Analog to digital converters (ADCs) for these applications require a low-supply voltage, low power consumption, 8-10 bits of accuracy, and an increasing demand on a high sampling rate [1,2]. The most recently reported single-channel CMOS ADCs with high sampling rate are compared in Fig. 1. Due to the possible tradeoff between speed, power dissipation, and die area, pipelined ADC architectures have been widely adopted to achieve the required performance [1]. Analog integration in deep submicron CMOS processes has become an economic necessity for many high-speed signal processing applications. This has brought several design challenges to the integrated analog circuits in purely digital submicron

technologies [3]. One of the most important challenges is the ability to build high DC gain amplifiers in these digital processes. Other major challenges relate to switch resistance issues. High gain and high speed are the two most important properties of the operational amplifiers (Op-Amps) used in pipelined ADCs. Op-Amps are the most critical block in those circuits. Fast settling requires a high gain-bandwidth-product, low parasitic capacitance, small devices, and no uncanceled low-frequency dipoles. High accuracy requires either a high DC gain or extreme linearity in the Op-Amp. New digital processes do provide fast and small devices with low supply voltage operation but at the cost of a relatively high threshold voltage and high output conductance. Traditional methods of enhancing DC-gain in the Op-Amps such as cascading, cascoding, and regulated cascoding are loosing their ability to provide sufficiently high DC gain due to the high output conductance of the digital transistors [4, 5]. Other non traditional approaches like the dynamically biased amplifiers suffer from slow settling problems [6]. Although design challenges can be reduced by using analog friendly low threshold voltage devices [2,3], this approach leads to increased fabrication costs, and extra processing steps. Moreover, analog friendly devices are leaky, their sizes are larger than the counter part digital transistors, and generally the analog friendly devices require increased power dissipation [3].

In this work, a 9bit 165MS/s pipeline ADC was built using all digital transistor Op-Amp. Positive feedback techniques have been adopted to get the high gain while using the digital transistors. In this case gain becomes partially dependent on matching between parameters of different devices and not on the absolute value of the parameters. Most of the previous positive feedback implementations have suffered from two problems: First is a strong dependence of amplifier gain on matching between different transistors parameters

where non of those parameters are controllable or have an inherent self tracking mechanism [4, 7]. Second is the high gain sensitivity to output signal swing, mainly because the feedback is traditionally taken from the output node that exhibits large swing. The implementation of a fast pipeline ADC with low supply voltage, low power dissipation, and an all digital transistors operational amplifier is described in the following sections.

## 2. Proposed Architecture

In this work, a 1.8V 9-bit pipelined ADC that can run as fast as 165MS/s is described. The block diagram of this ADC is shown in Fig. 2. The pipeline is constructed using four 3-bit stages. The first three stages have one bit of redundancy to provide relaxed requirements for the comparator and amplifier offsets. As shown in Fig. 2, the ADC is preceded by a switched capacitor programmable gain amplifier which also performs the sample and hold function. The ADC consists of three 3b multiplying analog to digital converters (MDACs), four 3b flash sub-ADCs, and supporting circuits that include non-overlapping clock generators and digital decoders. Each of the first three stages produce 3-bit codes, after the digital error correction (DEC) process the final ADC output word will be 9-bits long. The characteristic of the 3-bit MDAC stage is shown in Fig. 3 where one redundant bit is used for the DEC. A maximum comparator offset of $0.125V_{ref}$ can be tolerated. The voltage comparators have two stages, a pre-amplifier followed by a dynamic latch. An auto-zero technique is used for the voltage comparators to eliminate the offset effect as shown in Fig. 4 [8]. The MDAC circuit is shown in Fig. 5. The MDAC has gain of 4. For improved speed and linearity, one of the sampling capacitors ($C_{sf}$) is used as a feedback capacitor too by flipping it between input and output nodes. The sampling unit capacitor ($C_s$) has a size of 125fF. Fringing capacitors were used to realize the capacitors in the MDAC because they

have excellent matching properties, good linearity, and a high capacitance density. Input and output common mode voltages for the MDAC are the same. The input/output common mode reference voltage is generated internally. The 3-bit DAC threshold voltage levels, $\pm 0.75V_{ref}$, $\pm 0.5V_{ref}$, $\pm 0.25V_{ref}$, and 0 level were generated by connecting each of the three MDAC sampling capacitors either to $-0.25V_{ref}$, 0 , or $+0.25V_{ref}$ reference voltages.

Using an amplifier with open loop gain value equal to $A_{ol}$ and sub-ADC outputs the bits $D_1D_2D_3$. The MDAC gain can be written as

$$A_v \approx \left[\left(1+\frac{3C_s}{C_{sf}}\right)V_{in} - \frac{C_s\sum_{i=1}^{3}D_i}{C_{sf}}\frac{V_{ref}}{4}\right]\left(\frac{A_{ol}}{A_{ol}+1/\beta}\right); \quad D_i=-1,0,1; \quad \beta=\frac{C_{sf}}{C_{sf}+3C_s+C_{parasitics}} \qquad (1)$$

The main challenge in building this fast, low supply, low power, ADC is the design of the inter-stage amplifier. In very high speed applications parasitic capacitances of transistors at the amplifier's input/output nodes become an important factor that limits the settling speed. Digital transistors are smaller in size and thus have smaller parasitic capacitances than the analog friendly transistors. The fact that digital transistors have higher threshold voltages than analog friendly devices makes the difference in size for a specific current more significant. Since we are targeting a very high sampling rate, we chose to build the amplifier using all digital transistors. To enhance the speed further the chopped-diffusion transistor layout pattern shown in Fig. 6 was adopted. Chopping the transistor active area leads to a reduction in the diffusion parasitic capacitance at the expenses of increasing the side-wall capacitance which has a much lower density.

The two-stage amplifier architecture of Fig. 7a was built to achieve a high differential output swing of $1.1V_{p\text{-}p}$ while using a single 1.8V supply. The first stage is a new telescopic

cascode Op-Amp with positive feedback for gain boosting. The second stage is a simple differential pair. The positive feedback signal used to enhance the DC-gain is derived from the cascode nodes of the first stage. This feedback signal has a very low swing compared to the swing on the output node. Using this node as the sense node will substantially reduce the effect of the output voltage swing on the amplifier gain. For the rest of this work, different amplifier characteristics are derived for differential input differential output signals, even though, equivalent small signal circuits drawn will be only for one half of the amplifier.

The first stage of the amplifier has a simplified half circuit small signal model shown in Fig. 7b. Small signal analysis shows that the first stage has an open-loop gain, $A_v$, of the form:

$$A_v \approx \frac{g_{m1}\cdot(g_{o2}+g_{m2})g_{m3}}{[g_{o1}g_{o3}g_{o4}+g_{o2}g_{o3}g_{o4}+g_{o1}g_{o2}g_{m3}+g_{o3}g_{o4}g_{m2}-g_{o1}g_{o3}g_{m2}]} \tag{2}$$

This can be simplified to

$$A_v \approx \frac{g_{m1}g_{m2}g_{m3}}{[g_{o1}g_{o2}g_{m3}+g_{o3}g_{o4}g_{m2}-g_{o1}g_{o3}g_{m2}]} \tag{3}$$

Simplifying assumptions as $g_m >> g_o$ are made. Equation (3) shows that the DC-gain of the first stage becomes very large as ($g_{o1}\cdot g_{o3}\cdot g_{m2}$) approaches ($g_{o1}\cdot g_{o2}\cdot g_{m3}+g_{o3}\cdot g_{o4}\cdot g_{m2}$). To be more precise, achieving this equality makes the gain of the amplifier comparable to what would be achieved with a double cascode structure that would require the stacking of two additional transistors in each half-circuit. It is well known that the channel length modulation causes the transistor output conductance to be larger than zero [16]. The transistor output conductance is given by

$$g_{oi}=\lambda_i I_{dsi} \tag{4}$$

where $\lambda i$ is the channel length modulation coefficient and $I_{ds}$ is the common drain current. It is well known that the $\lambda$ parameter is dependent on gate length and is given by the relationship [16]

$$\lambda_i = \frac{1}{L_i} \cdot \frac{\partial X_{di}}{\partial V_{dsi}} \tag{5}$$

where $X_d$ is the gate reduction of the channel due to $V_{ds}$. If it is assumed that $(dX_{di}/dV_{dsi})$ is constant and the same for both N-channel and P-channel devices, If we choose the lengths $L_1$, $L_2$, $L_3$, and $L_4$ so that $L_1=L_3$, and $L_2=L_4$, then

$$\frac{1}{L_1 \cdot L_2} + \frac{1}{L_1 \cdot L_2} - \frac{1}{L_1^2} = 0 \tag{6}$$

which will be satisfied if

$$L_2=2L_1 \tag{7}$$

Thus, setting $L_2=2L_1$ will result in the gain given by

$$A_v \approx \frac{g_{m1} \cdot g_{m2} \cdot g_{m3}}{[g_{o1}g_{o3}g_{o4} + g_{o2}g_{o3}g_{o4}]} \tag{8}$$

assuming $g_{m1}=g_{m3}$ and substituting from (5),(6) and (7) into (8) we obtain

$$A_v \approx \frac{2g_{m1}^2 \cdot g_{m2}}{3g_{o1}^2 g_{o4}} = \left[\frac{g_{m1} \cdot g_{m2}}{2g_{o1}^2}\right]\left[\frac{4g_{m2}}{3g_{o4}}\right] \tag{9}$$

It can be shown that the gain of the basic cascode without the positive feedback is given by

$$A_v \approx \frac{g_{m1} \cdot g_{m2} \cdot g_{m3}}{[g_{m3}g_{o1}g_{o2} + g_{m2}g_{o3}g_{o4}]} \tag{10}$$

If we assume $g_{m2}=g_{m4}$ in this structure and the lengths are all the same so that $g_{o1}=g_{o3}=g_{o2}=g_{o4}$, then the basic cascode has gain of

$$A_v = \frac{g_{m1} \cdot g_{m2}}{2g_{o1}^2} \tag{11}$$

Comparing (9) and (11), it follows that the positive feedback and length sizing has resulted in a boost in gain of $(4g_{m2}/3g_{o4})$ which can be quite significant.

The common mode circuit of the first stage can be redrawn as shown in Fig. 7c. To see how process variations will affect the quiescent voltages and currents of the circuit, let us consider the strong PMOS case. For this case, the magnitude of $V_{th}$ for the PMOS transistors will be lower resulting in larger $g_{o3,4}$ and $g_{m3,4}$ since transistors $M_3$ and $M_4$ are connected to fixed bias references. Therefore, both the nodes $V_{out\_T}$ and $V_x$ will be pulled up towards $V_{dd}$. Since the operating point of the transistor $M_2$ is set by the positive feedback connection, and since $M_2$ forms an inverting common source amplifier with source degeneration, then increasing its $V_{gs}$ will turn it on harder increasing $g_{m2}$, $g_{o2}$, and $g_{o1}$. Since $g_{o1,3}\approx 2g_{o2,4}$ this will make the increase in the value of the negative term in the denominator of Eq. (3) able to track the increase of the sum of the positive terms and adjusting the gain. Note that the change in the excess bias of transistor $M_3$ is equal to the change of the excess bias of transistor $M_2$ which helps $g_{m2}$ and $g_{m3}$ to track each other under the assumption of fixed voltage at node $V_y$. This negative feedback loop in the common mode circuit, shown in Fig. 7c, has a large gain and its operation is consistent with the operation of the common mode feedback circuit. Similar arguments can be made for the other process corners. The existence of the extra biasing circuitry, shown in faded color in Fig. 7a has two main functions: First, it defines the

quiescent biasing voltage, $V_y$. Second, it helps to fix the voltage of node $V_y$. Observing voltages $V_x^{\pm}$ we notice that they experience very small swings compared to $V_{out}^{\pm}$, since

$$V_x^{\pm}=V_{out}^{t}/(g_{m3}/g_{o3})/G_s \tag{12}$$

where $G_s$ is the gain of the common source output stage. For example in our design $(g_{m3}/g_{o3}* G_s)>200$, so if the differential output voltage has a swing of $1V_{p\text{-}p}$, then voltage $V_x^{\pm}$ will experience less than $5mV_{p\text{-}p}$ swing. Therefore, the feedback is almost unaffected by the output signal level. The two stages amplifier is Miller compensated. Compensation capacitors ($C_{C1}$, $C_{C2}$) where connected to the cascode nodes, for simplicity, only one side of the compensation capacitors is shown in Fig. 7a.

## 3. Simulation Results

The proposed ADC and amplifier were simulated using Texas Instruments digital 0.21μm CMOS process. Each amplifier in the ADC draws a total current of 6.5mA. All simulation results presented are for differential signals. An AC analysis shows that the amplifier has a DC gain of 81dB with a unity gain frequency of 1.218GHz while driving a 1pF load. Results are shown in Figure 8. The phase response is shifted up by 180 degrees to give a direct reading for the phase margin. Fig. 8 shows a comparison between the AC analysis of the proposed amplifier and the traditional telescopic amplifier followed by the common source amplifier built using all digital transistors under the same conditions. AC analysis shows that we where able to enhance the DC gain from 64dB to 81dB without sacrificing the bandwidth or phase margin. The DC sweep in Fig. 9 shows that the amplifier has a maximum swing of $1.5V_{p\text{-}p}$ while maintaining a gain higher than 68dB under nominal conditions. Layout extraction shows that by using the chopped diffusion pattern for wide

devices we can save 15% to 20% of the parasitic capacitance value. Extensive post layout transient simulation for the whole ADC at 165MS/s was performed. A typical simulation result for the first stage output is shown in Fig. 10 where the sampling unit capacitor, $C_s$, of Fig. 5 has a size of 125fF. Simulation shows that the amplifier was able to slew and settle to an error less than 0.2mV for a 1V peak-to-peak output swing within 2.1nsec. Due to the use of digital transistors as switches in the common mode feedback circuit, a memory effect, incomplete reset, may appear by sampling at higher frequencies.

## 4. Test Results

The prototype 9-bit 1.8V pipelined ADC was fabricated in a 0.21μm, 5 metal layer, double poly, CMOS copper technology. A die photo of the ADC is shown in Fig. 11. The die surface was covered with dummy metal layers thus obscuring most relevant details. The total die area for the ADC, a front end programmable gain amplifier (PGA), and a reference amplifier is 711μm X 743μm. The input/output swing of the MDAC is $1.1V_{p\text{-}p}$. The ADC was tested at different sampling speeds. The measured DNL/INL was 0.305/0.7LSB, 0.33/1.03LSB, and 0.87/1.8LSB at 27MS/s, 80MS/s, and 165MS/s respectively. The measured DNL and INL curves at 165MHz are presented in Fig 12. Test results at different sampling speeds are listed in Table 2. Sampling errors due to switch resistance became apparent at 165MS/s. The measured total power dissipated in the ADC was 90mW at 165MS/s and 1.8V supply voltage. This ADC has the lowest reported power dissipation for a fast pipeline ADC with this range of resolution [2, 7-10]].

The ADC dynamic performance is evaluated by measuring signal to noise and signal to noise plus distortion ratios (SNR and SNDR) in addition to measuring the spurious free dynamic range (SFDR). The measured SNR, SNDR, and SFDR at 165MS/s were 44.3dB,

44dB, and 57dB respectively. SNR measurement for a 0.5V sinusoidal input is shown in Fig. 14. Summary of other measurements appear in Table 2.

Table 2. Summary of ADC performance measurements

| Resolution | 9-bits | | |
|---|---|---|---|
| Process | 0.21μm, 2 poly, 5 metal, CMOS | | |
| Power Supply | Single ended 1.8V | | |
| Total Power | 90mW | | |
| Die Size | 711μm X 743μm | | |
| Sampling Freq. | 27 MS/s | 80 MS/s | 165MS/s |
| Max swing | 1.1 $V_{pk\text{-}pk}$ | 1.1 $V_{pk\text{-}pk}$ | 1.1 $V_{pk\text{-}pk}$ |
| DNLmax | 0.305 LSB | 0.333 LSB | 0.87 LSB |
| INLmax | 0.706 LSB | 1.026 LSB | 2.7 LSB |
| $SNR_{dB}$ | 48.193dB, $f_{in}$=6MHZ | 46.78dB, $f_{in}$=10MHz | 44.48dB, $f_{in}$=10MHz |
| $SNRD_{dB}$ | 47.9dB | 46.3dB | 44dB |

As shown in Fig. 1, the ADC presented in this paper shows the fastest sampling speed, and the lowest power dissipation among the previously reported high performance pipeline ADCs. In fact, this work is the first to report building a high gain Op-Amp using all digital transistors. Moreover, This is the first work to claim gaining around 20 dB in gain where the gain is robust and insensitive to temperature variations, process variations, and wide output signal swings. In combination with bootstrapped switches, this novel amplifier architecture opens the door to building high performance ADCs in pure digital low supply, CMOS processes without the need of the expensive analog friendly devices.

## 5. Conclusions

A 1.8V, 9b low power, pipelined ADC was built using an all digital transistors opamp in a 0.21μm CMOS copper technology. Test results show no missing codes at sampling rate of 165MS/s. An energy efficient fast settling positive-feedback technique with self-adaptive

gain adjustment and very low gain sensitivity to output swing was used to build the opamp. A special chopped diffusion transistor layout technique was adopted to reduce the parasitic capacitance at the important nodes.

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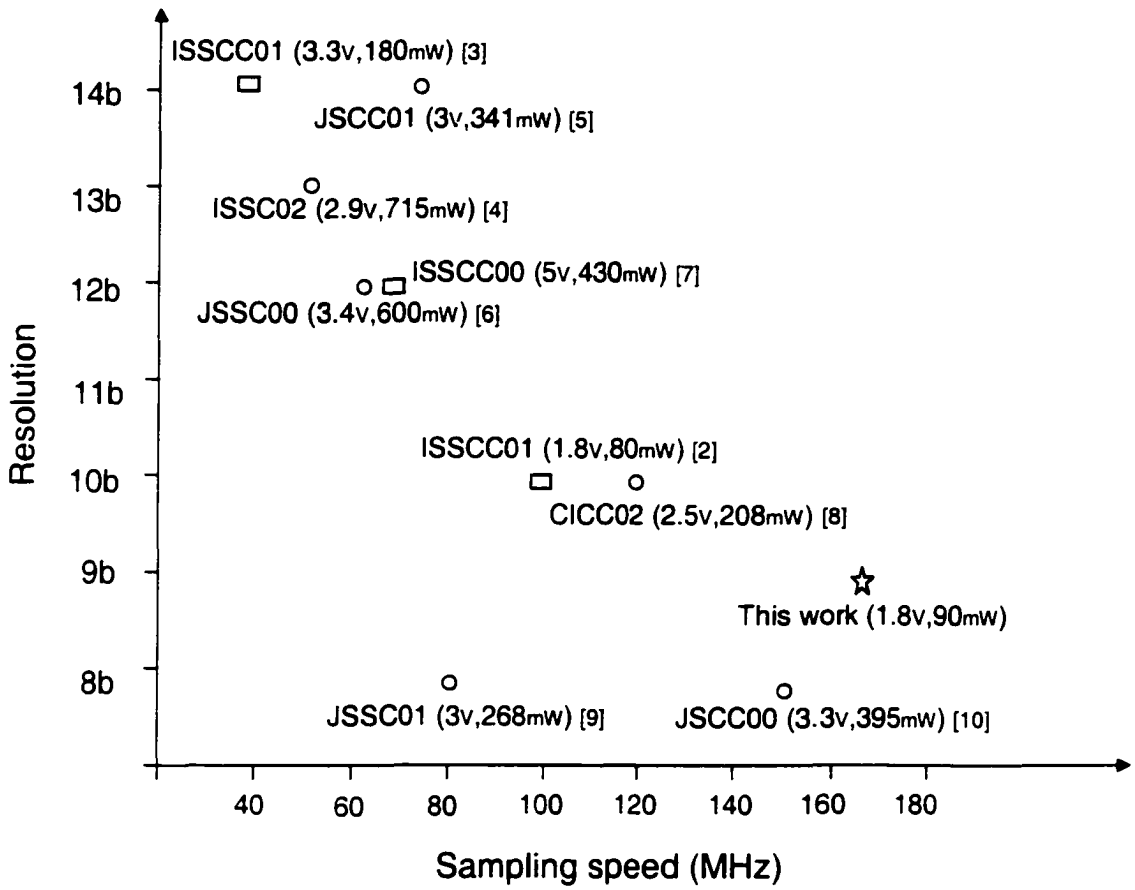



Fig. 1 Previously published fast CMOS pipeline ADCs.

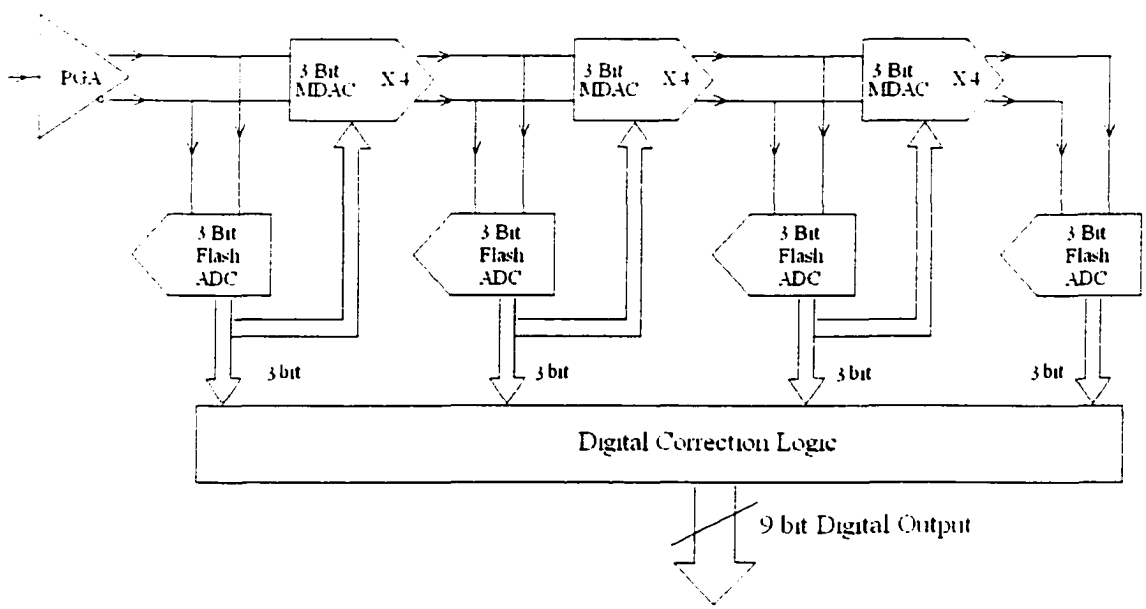



Fig. 2 ADC block diagram.

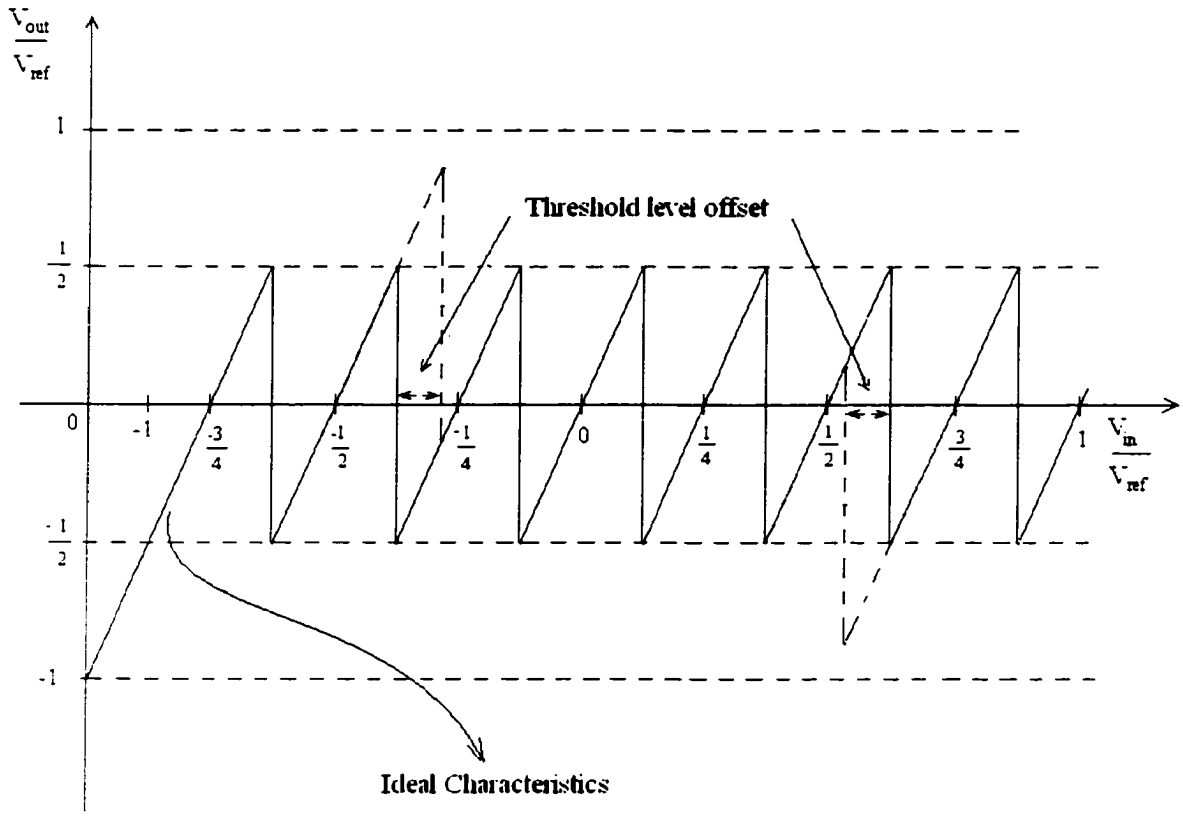



Fig. 3 MDAC characteristics with one redundant bit.

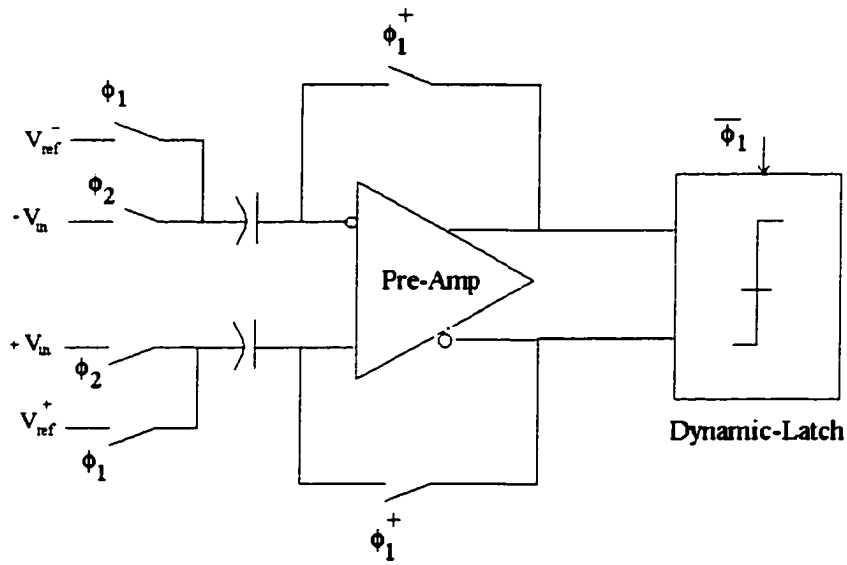



Fig. 4 Voltage comparator block diagram.

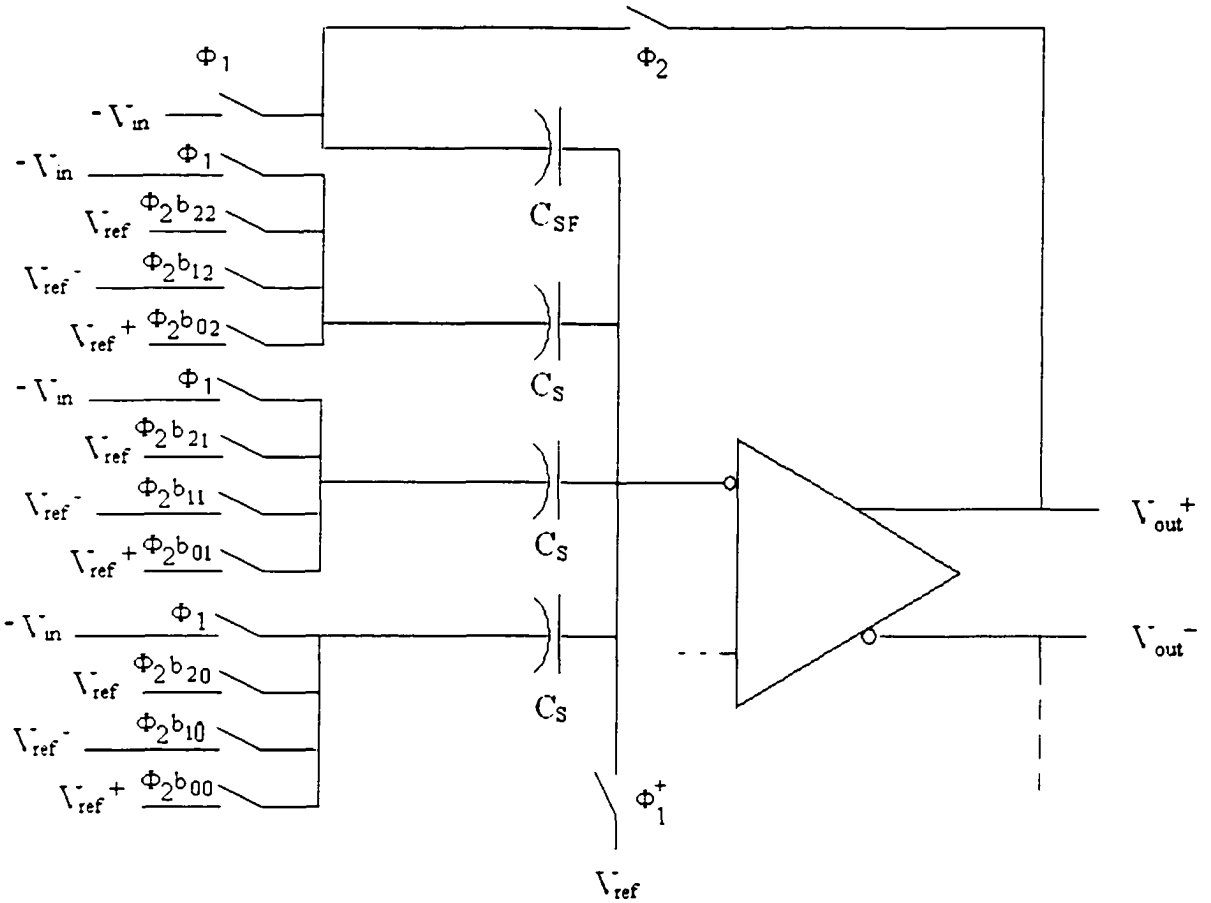



Fig. 5 A 3-bit MDAC circuit.

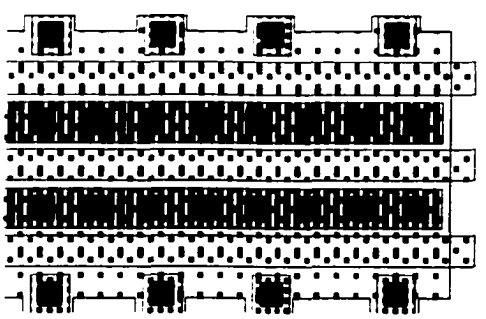


Fig. 6 Chopped-diffusion transistor-layout pattern.

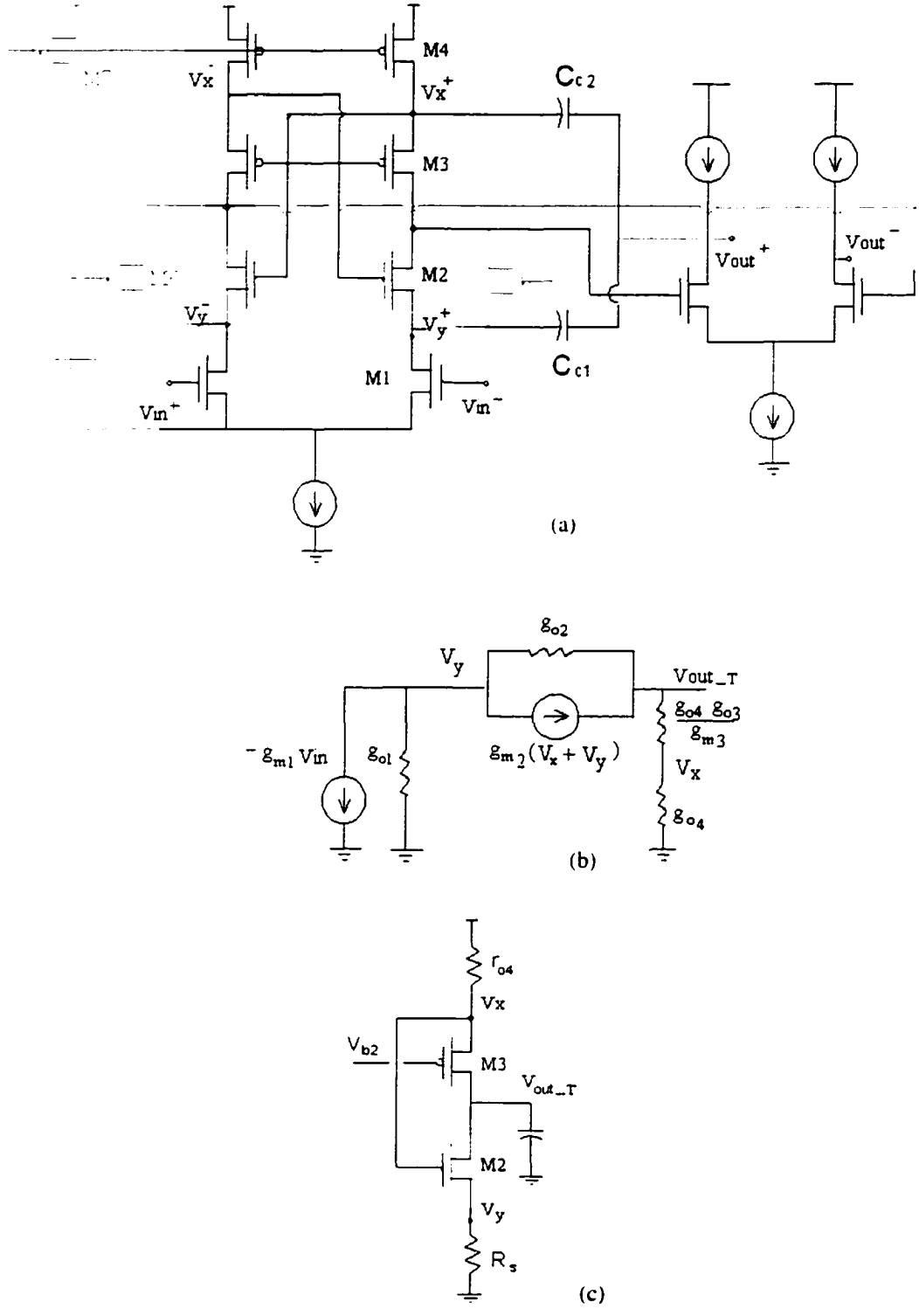



Fig. 7. Proposed amplifier with positive feedback. (a) Amplifier schematic. (b) Small signal model of one side of the 1st stage of the amplifier. (c) Simplified schematic of the common mode of the 1st stage amplifier.

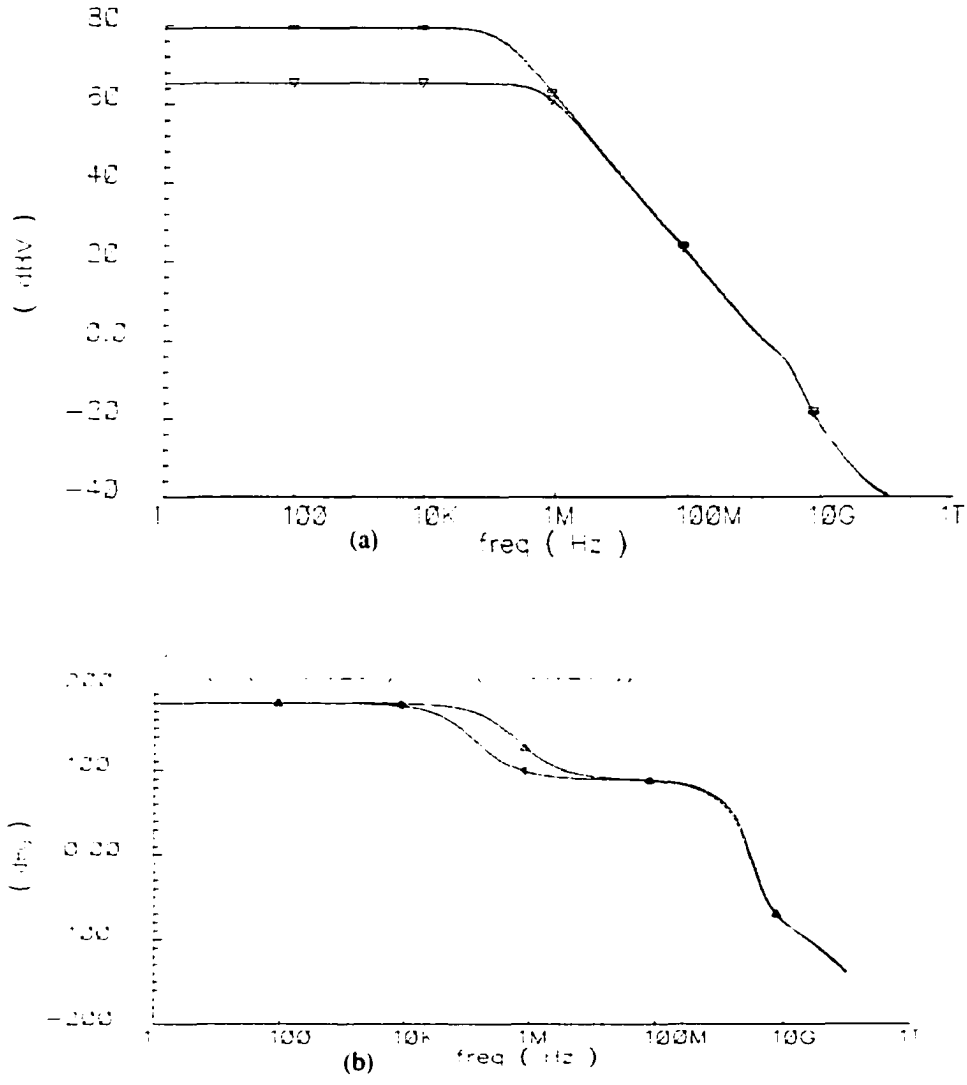



Fig. 8. AC characteristics of the amplifier with and without positive feedback. (a) Magnitude response. (b) Phase response.

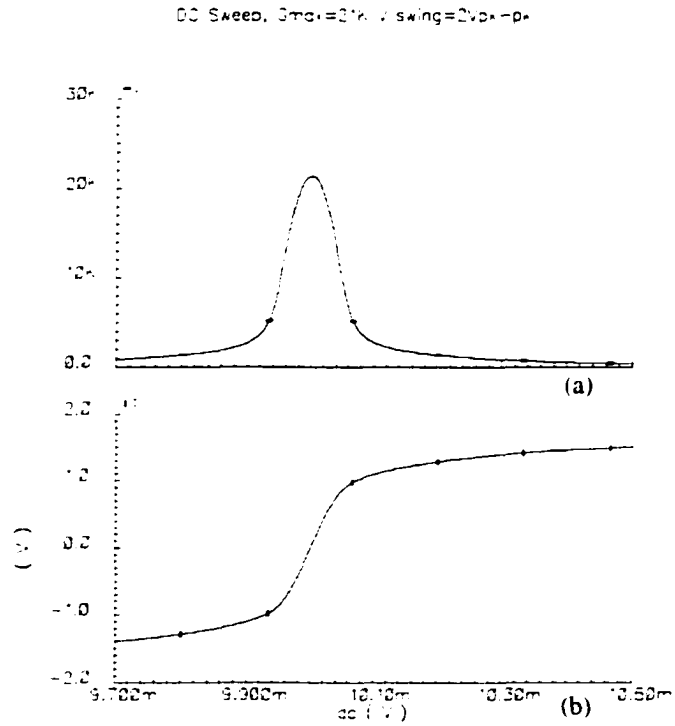



Fig. 9. DC sweep of the proposed Op-Amp. (a) Gain vs. input swing. (b) Input/Output characteristics.

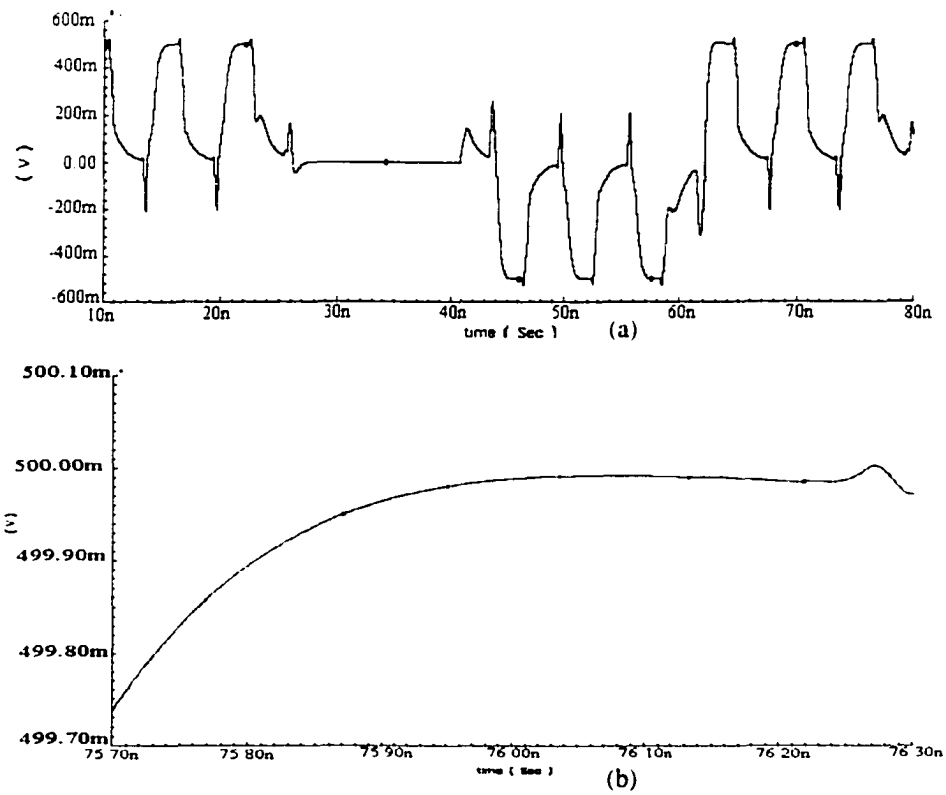



Fig. 10. MDAC differential output. a) Flipping between extreme outputs. b) Zoomed settling.

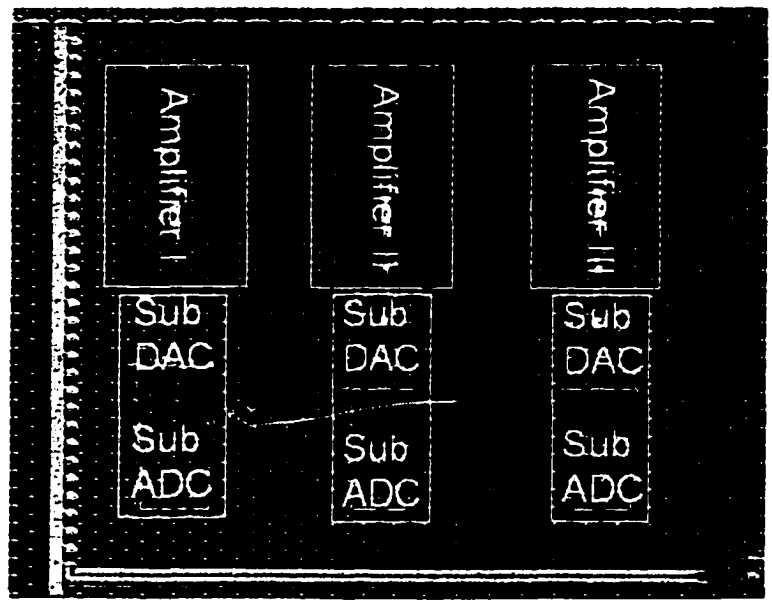



Fig.11 Die photo of a 9-bit pipeline ADC.

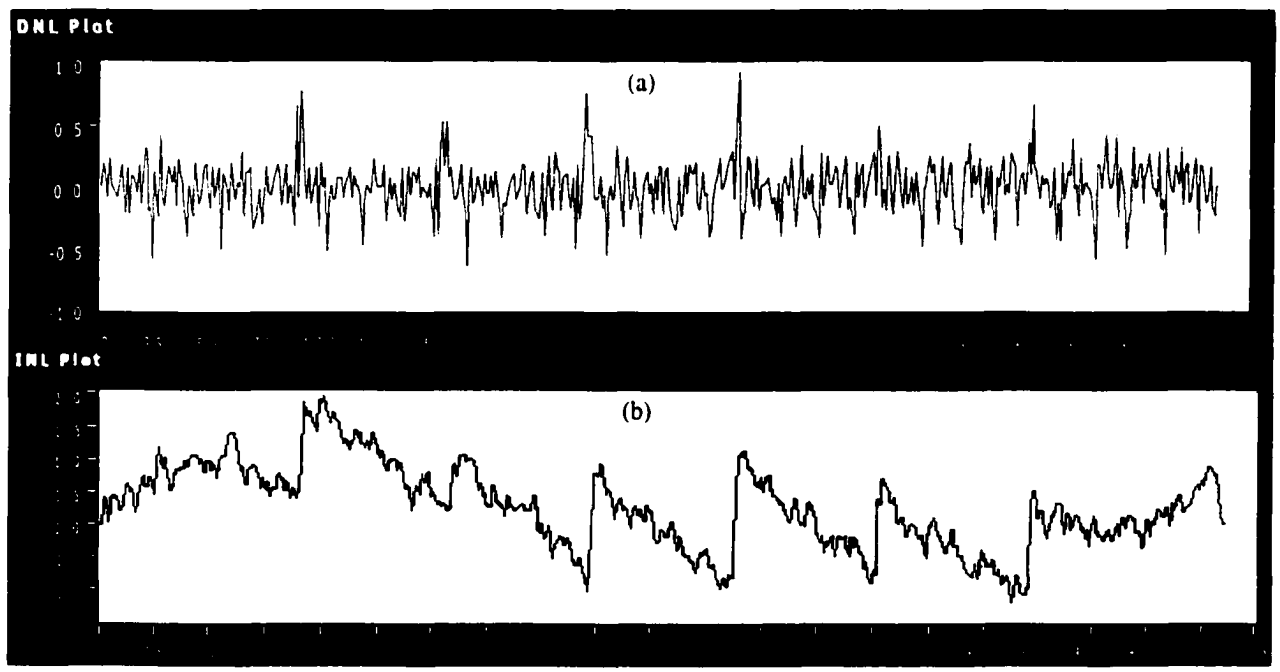



Fig. 12 Linearity measurements for the ADC at 165MS/s. (a) Measured DNL. (b) Measured INL.

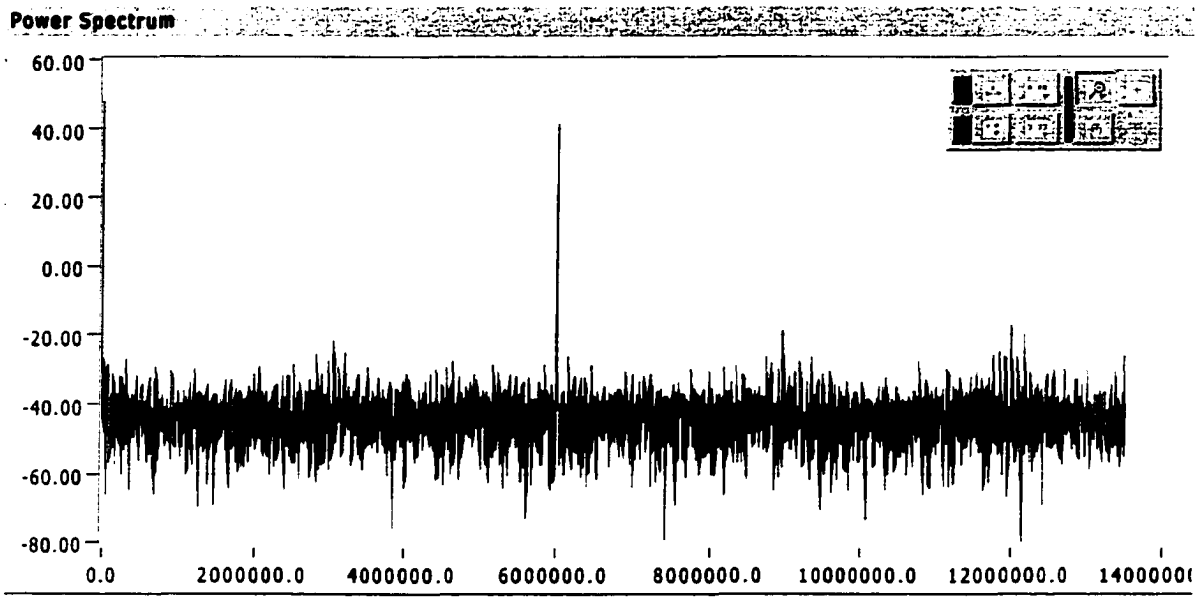



Fig. 13 Measured signal to noise ratio (SNR) for 10MHz input frequency and 165MS/s sampling rate.

# CONCLUSIONS

There is an increasing demand on signal processing being performed on chip with an increasing demand on sampling speed. Recently there is a wide employment of the sub-micron digital CMOS processes in the industry. The adoption of the digital CMOS processes has brought new challenges to the analog design area. The most important challenge is the ability to build high gain amplifiers. Other important challenges relate to switch ON-resistance exist. Traditional gain enhancement techniques including cascading, cascoding, and regulated cascoding are loosing their ability to provide high gain amplifiers while maintaining wide swing, high speed, and low supply voltage operation. Expensive solution represented by building special analog friendly devices on the expense of extra fabrication processing steps is used most of the time.

Positive feedback technique, also known as negative conductance, or Bootstrapping technique, can provide us with high DC gain amplifiers since the gain becomes more dependent on matching of parameters of different transistors rather than on the absolute value of the parameters. Further more, new digital processes have much better matching properties compared to older processes. A survey of the previous positive feedback implementations shows that it has the following advantages

- High DC-gain is possible, even with high output conductance devices.
- No speed penalty, no additional poles.
- Applicable to low voltage processes/systems.

On the other hand previous implementations have shared the following points of concern

- Perfect matching is required to achieve very high DC-gain.

- Gain is very sensitive to the output voltage level, swing.

In this work, we have investigated a new way of implementing the positive feedback technique in conjunction with one level of cascoding. Cascoding will provide us with more gain and extra nodes that exhibit the same output nodes signal characteristics but with much reduced swings. So cascode nodes can be used to draw signals for the positive feedback loops. During this thesis we presented several novel architectures that uses either a fully controllable positive feedback scheme, where some parameters are easily controlled by controlling some biasing currents on the expense of the replica biasing scheme, or architectures with self-tracking parameters, so sufficiently high gain can be maintained across processes and temperature corners without the need for extra gain-control circuit. The use of the cascode nodes to generate the positive feedback rather than the wide swing output nodes makes amplifier gain exhibit reduced sensitivity to the output signal swing.

New architectures that use the biasing and cascode transistors as amplifying transistors in conjunction with positive feedback technique are studied. It is shown that speed, transconductance, and gain enhancement can be performed without penalty in dissipated power and signal swings, but on the expense of more design complexity. An implementation on a high Q-factor, high center frequency bandpass filter is presented.

Finally an ultra fast 9bit, 1.8V, 165MS/s, low power, pipeline ADC that uses all digital-transistors positive feedback wide swing amplifier is designed, fabricated, and tested on 0.21μm digital CMOS process. Test results proved the claimed advantages of this proposed work.

# APPENDIX A: LAYOUT AND TESTING TIPS

The layout of the chip is becoming a very critical factor in determining the implemented system performance. For example, matching of transistors at the input differential stage will determine the amplifier or the comparator offset voltage. Matching of capacitors in the multiplying digital to analog converter (MDAC) will affect the accuracy, i.e. gain error. Layout pattern of transistors across the output nodes will affect slewing and settling speed. Moreover, the technology used will affect the layout patterns that can be used. For example as we go deep in sub-micron processes, spatial dimensions are shrinking down while vertical dimensions are almost the same. So it became more feasible to use the fringing capacitors in those sub-micron processes. On the other hand, mutual capacitance and cross talk between connecting lines is boosted.

While doing the layout of the ADC, and for the amplifier, the chopped diffusion layout pattern, shown in Fig. 1, has been adopted for transistors across the output nodes of the first and the second stages. To avoid cross talk between the clock lines and signal lines, digital and clock nets are placed away from the amplifier layout. The ADC layout floor plan is shown in Fig. 2. Clock lines and signal lines are totally separated. Switches connected to the signal path have double guard rings around them. Moreover PMOS transistors are packed together toward the high supply voltage, while NMOS transistors are packed together toward the ground contacts bus. All the transistors in the amplifier are cross coupled in a mirror image form as shown in Fig. 3. Dummy devices have been added for the NMOS transistors in the differential pairs of the first and second stages. Fringing capacitors have been used to realize the MDAC and the compensation capacitors where four metal layers have been

involved in each capacitor as shown in Fig. 4 for two layers. Nine capacitors were built where only eight capacitors have been used by the MDAC, four capacitors in each side, the final one is a dummy capacitors for full symmetry as shown in Fig. 5. The final ADC channel layout is shown in Fig. 6.

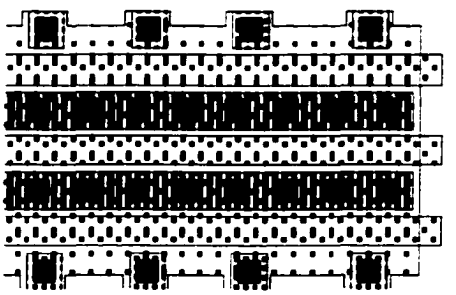


Fig. 1 Chopped-diffusion transistor layout-pattern.

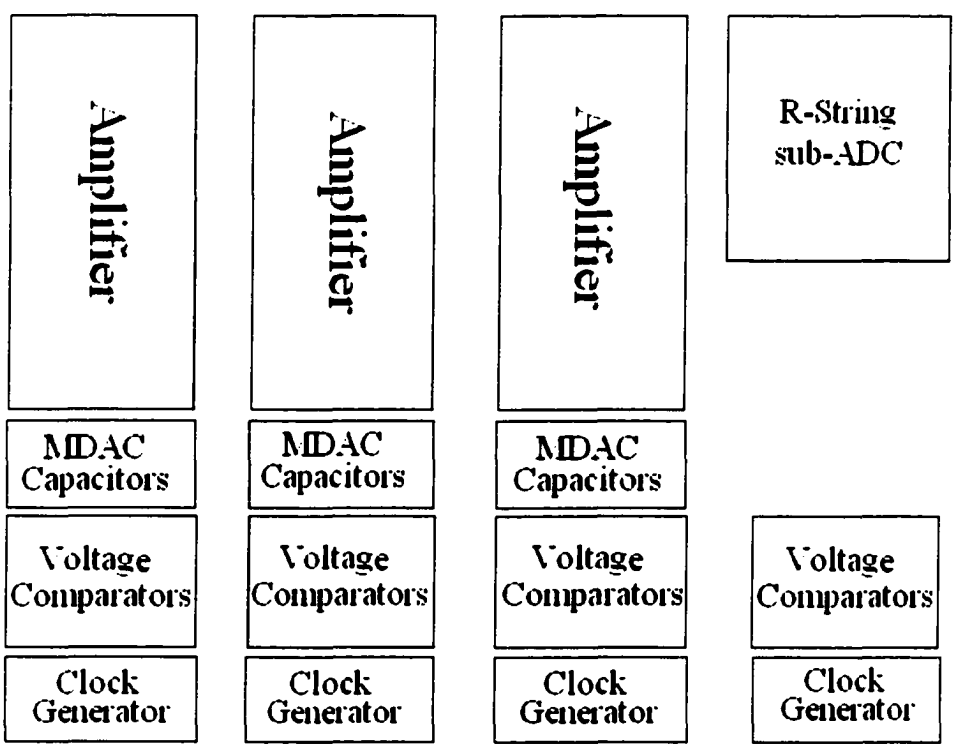



Fig. 2 ADC layout floor-plan

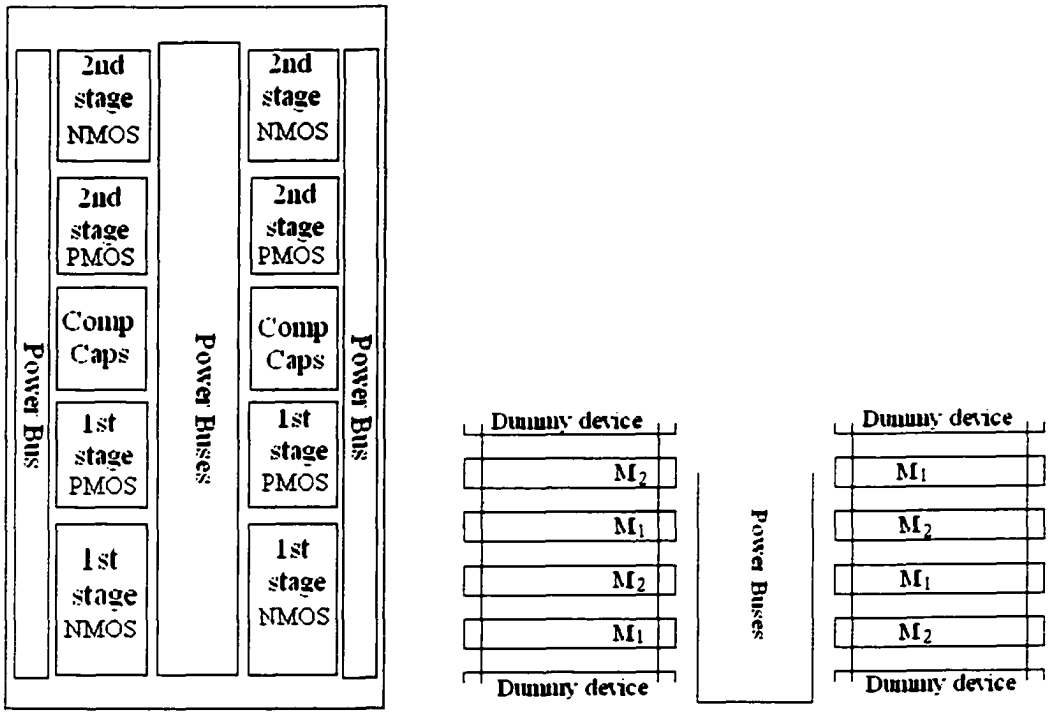



Fig. 3. a) Amplifier layout floor-plan. b) Zoomed differential pair input transistors layout

Fig. 4 Fringing capacitors, a) top view, b) two layers view.

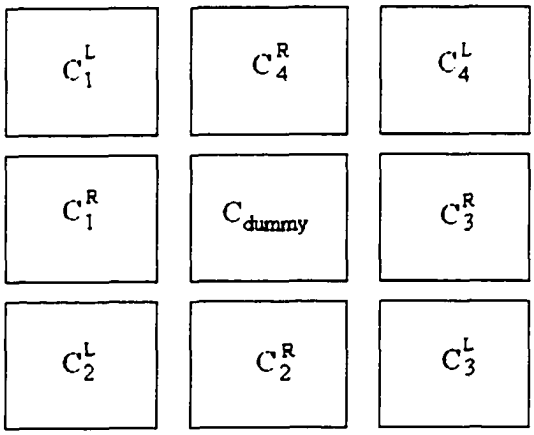



Fig. 4c. MDAC capacitors layout.

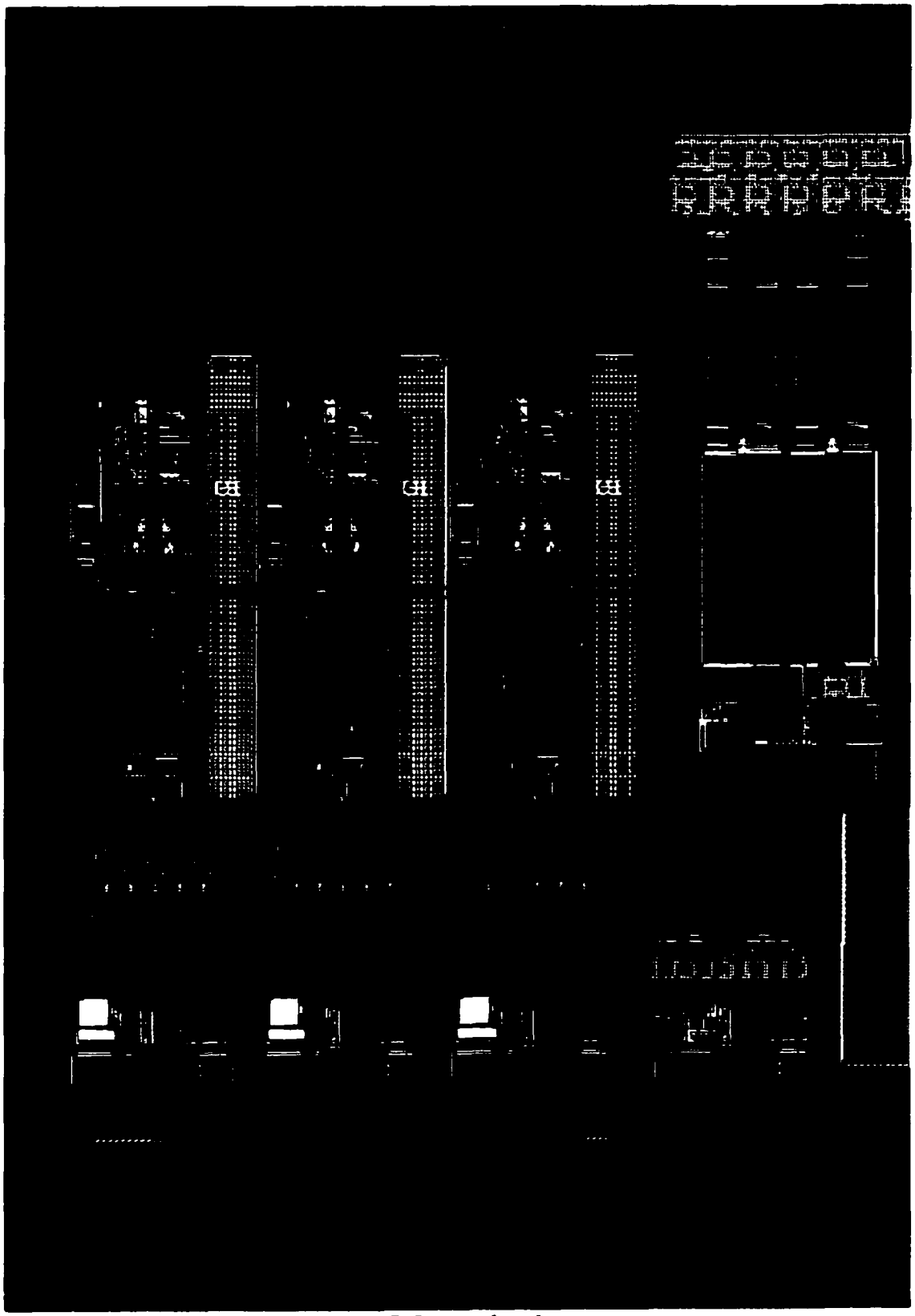


Fig. 5 ADC complete layout.

Testing for the ADC was done in two steps: Linearity testing, and dynamic performance testing. The linearity testing was based on the statistical approach where a very fine linear signal generated using a high accuracy, 18 bit, sigma-delta DAC was applied to the ADC input. The input has a form of a periodic triangular wave with equal rise and fall times, i.e. slopes. If the ADC operates ideally then all the ADC output codes should have the same probability of occurrence. The Histogram of the generated codes is plotted, in our case each code is to be generated fifty times per bin (50 code hits/bin). In real testing the triangular input signal exceeds the ADC input range this is why the ADC output capture waveform shows clipped triangular wave as shown in Fig. 6.a. If all the codes show up at the ADC output capture waveform with a minimum acceptable probability then this means no missing codes. A code is defined as missing if its probability of occurrence is less than 1/10 times the ideal probability of occurrence for that code.

For the clipped ADC output signal if we exclude the first and last codes, then all the codes have equal probability of occurrence given by

$$P_{any\ code} = (1 - P_{first\_code} - P_{last\_code})/(\text{total\_codes} - 2) \quad (1)$$

Due to linearity imperfections some codes will appear more frequently than other codes. Since linearity is related to the code interval width, ideally all codes have the same interval width, the deviation of the probability of occurrence of a certain code from its ideal value becomes a direct measure of the deviation of that code interval width from its ideal value. Thus the normalized deviation of the probability of occurrence of a certain code from it ideal value is called the Differential Non-Linearity (DNL) at that code. So at code[n], the DNL is

$$DNL[n] = \frac{code[n]\_count \bullet (ADC\_codes - 2)}{(total\_samples - last\_code\_count - first\_code\_count)} - 1 \quad (2)$$

DNL errors accumulate over a series of codes and cause a total deviation from the ideal transfer curve, characteristics. The integral none linearity (INL) at code[n] is derived as

$$INL[n] = \sum_{k=0}^{n-1} DNL[k]$$

So the INL and the DNL can be estimated based on the estimation of the probability of occurrence for each code. For accurate probability estimation, large number of samples should be captured. A rule of thumb, the number of samples captured should be two orders of magnitude higher than the number of codes in the ADC.

Fig. 6 shows the linearity testing procedure. Fig. 6.a shows the ADC output captured waveform for the sweep 0.5V input. Fig. 6.b shows the generated histogram that shows the number of generated codes per bin. Fig. 6.c shows the generated DNL[n] plot generated using the statistical approach. Finally Fig. 6.d shows the estimated INL[n].

Finally the dynamic performance is measured by measuring the signal to noise ratio (SNR), signal to noise and distortion ratio (SNDR), and the supuriouse free signal to distortion ratio (SFDR). All those measurements are done by applying a fast pre-filtered sine wave input to the ADC and using the spectrum analyzer to measure the harmonics an example of measured SNR and SNDR is shown in Fig. 7.

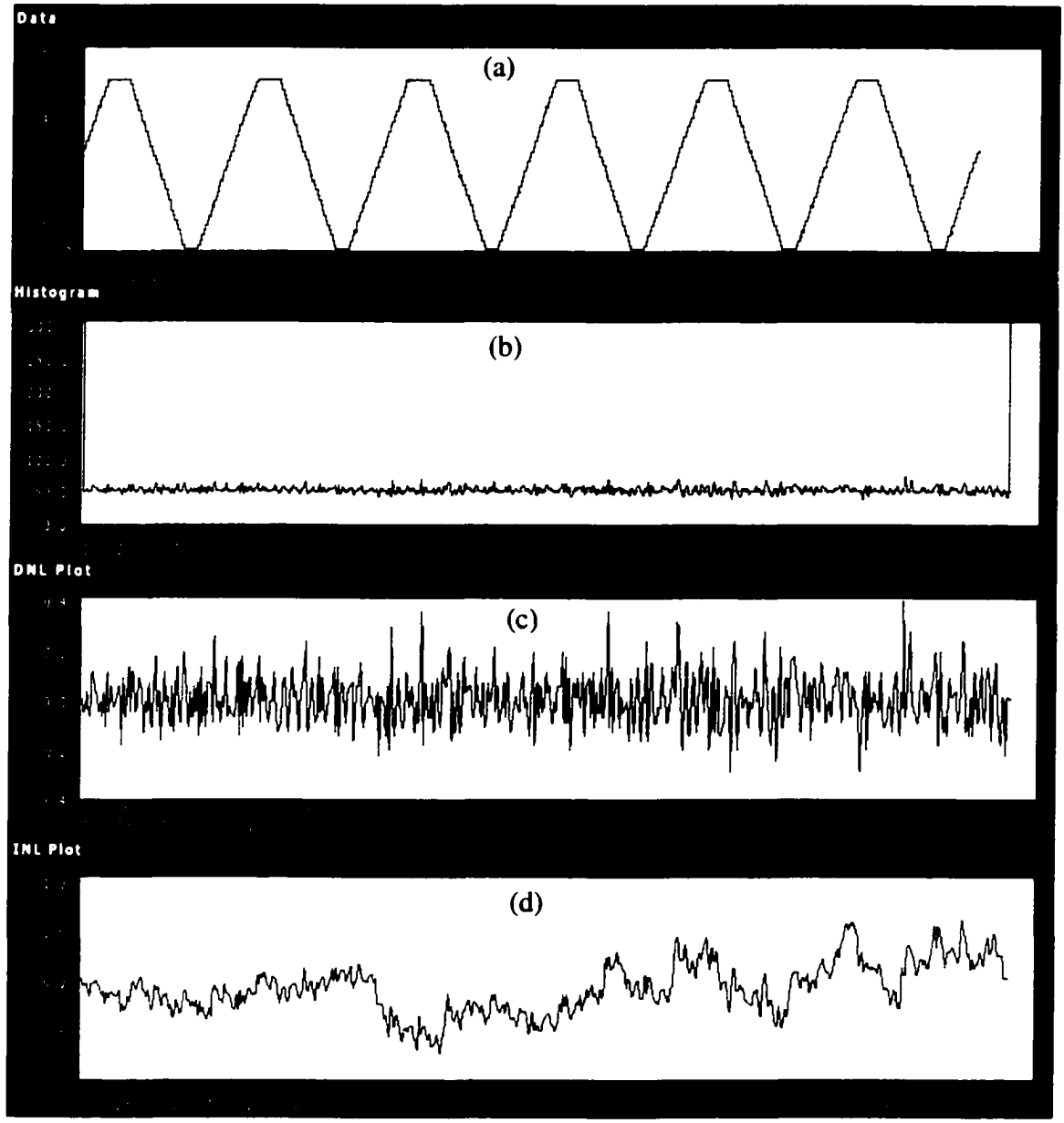



Fig. 6. Linearity testing steps. (a) ADC output captured waveform. (b) Histogram. (c) DNL plot. (d) INL plot.

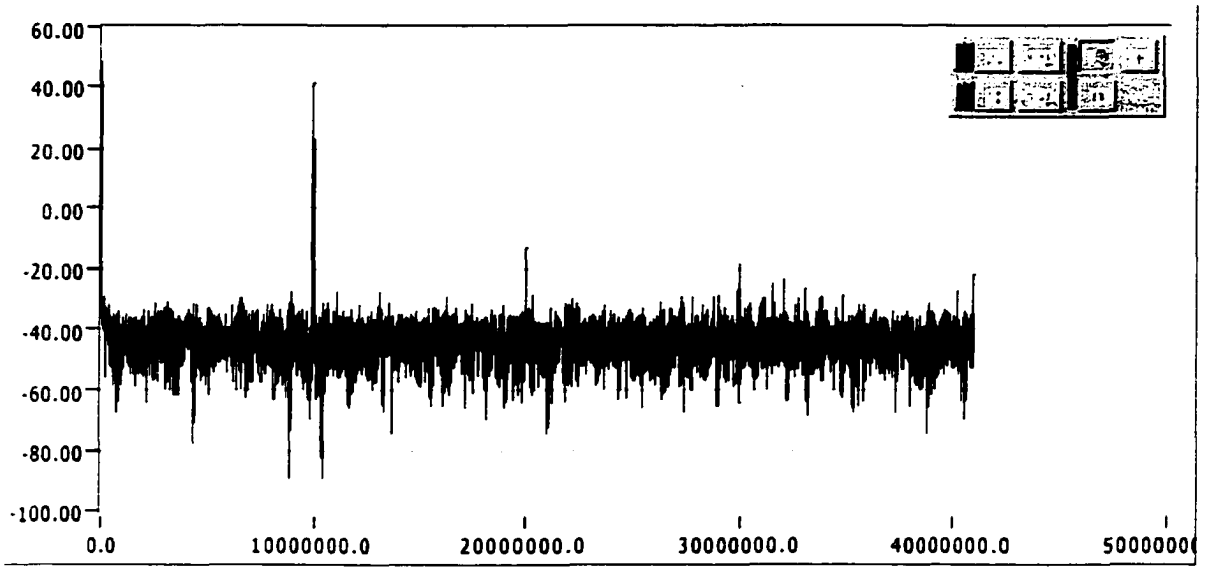
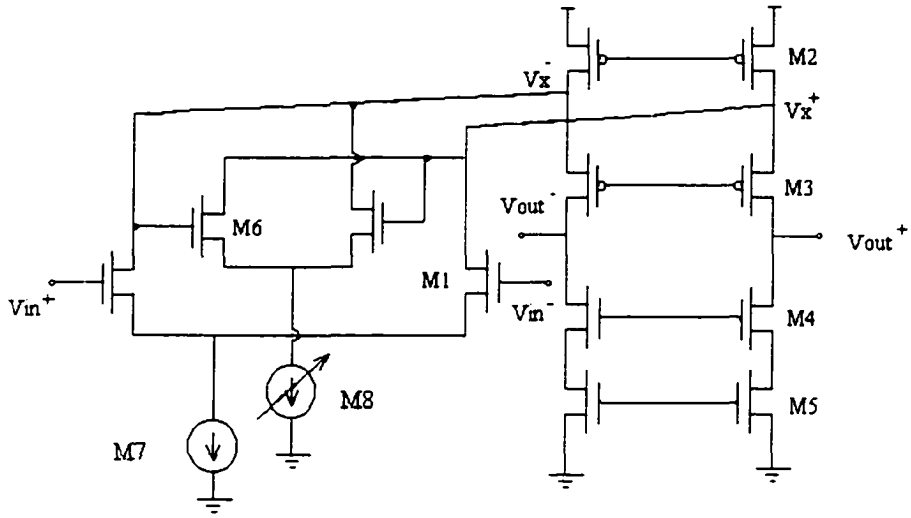
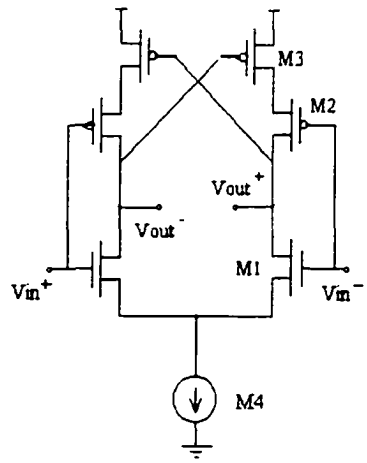



Fig. 7. Testing of the signal to noise ratio (SNR) for 10MHz input freq and 82MS/s.

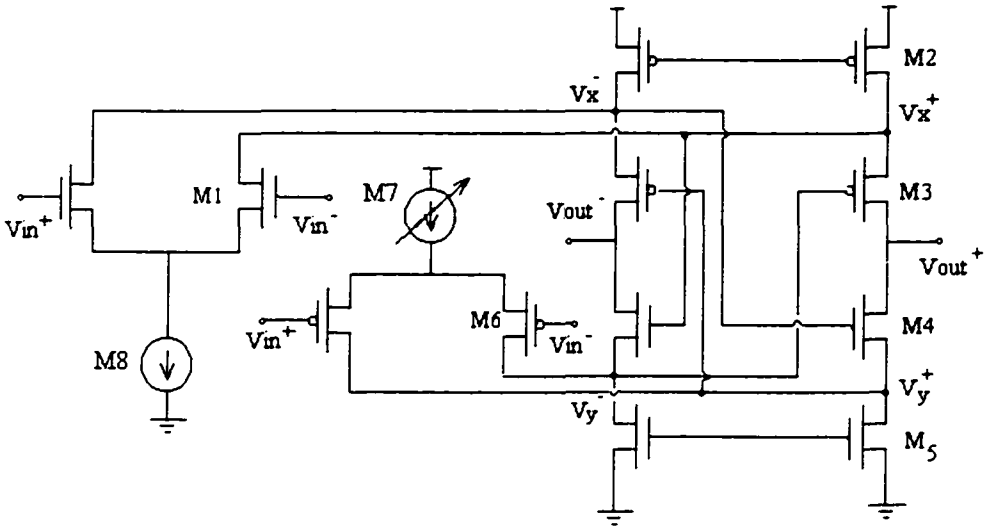
# APPENDIX B: LIST OF AMPLIFIERS AND THEIR TRANSISTOR SIZES



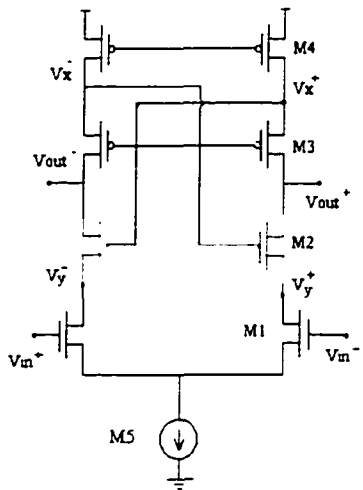

| Transistor | M1 | M2 | M3 | M4 | M5 | M6 | M7 | M8 |
|---|---|---|---|---|---|---|---|---|
| W/L (μm/μm) | 7.2/0.25 | 23.4/0.36 | 20/0.25 | 4.8/0.25 | 9.6/0.6 | 0.88/0.25 | 8.8/0.6 | 0.8/0.36 |




| Transistor | M1 | M2 | M3 | M4 |
|---|---|---|---|---|
| W/L (μm/μm) | 6/0.24 | 6/0.24 | 1.2/0.36 | 6.8/0.48 |




| Transistor | M1 | M2 | M3 | M4 | M5 | M6 | M7 | M8 |
|---|---|---|---|---|---|---|---|---|
| W/L (μm/μm) | 2.7/0.25 | 17.3/0.36 | 15/0.24 | 3.9/0.25 | 4.32/0.36 | 8.8/0.25 | 32/0.6 | 9.6/0.6 |




| Transistor | M1 | M2 | M3 | M4 | M5 |
|---|---|---|---|---|---|
| W/L (μm/μm) | 51.1/0.245 | 72.45/0.42 | 116/0.21 | 245.77/0.42 | 266/0.42 |